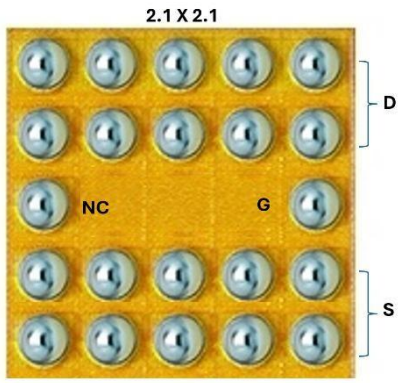
5mΩ 40V in GBA

Description

This is a 40V GaN-on-Si enhancement-mode power transistor. The properties of GaN allow for high current and high switching frequency at high power density.



Applications

- High-Frequency DC-DC Converters (Non-Isolated)
- LiDAR (Laser Drivers)
- Class-D Audio Amplifiers
- Motor Drives (Low Voltage, High Performance)
- Power over Ethernet (PoE) & Battery Protection

Features

- 40V Bi-directional blocking capability
- Ultra low on-resistance
- Reverse current capability
- GaN-on-Silicon E-mode HEMT technology
- RoHS, Pb-free, REACH-compliant

Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
V_{DD}	40	V
$R_{D1D2(on)}$,Typ @V_G=5V	5	mΩ
QG,typ @ V_{DD} = 20 V	16	nC
ID (TC=25℃)	20	A

Table2 Ordering Information

Ordering Code	Type	Product code
GPLVR050B2	**BGA**	**GPLVR050B2**

Table of Content

1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. **Table 3 Maximum rating**

Parameters	Symbols	Values	Units	Notes/Test Conditions
Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage	V_{DD}	40	V	V_{GD1} = 0 V or V_{GD2} = 0 V Tj = -40℃ to 125℃
Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage(transient)	$V_{DD,\ transient}$	60	V	V_{GD1} = 0 V or V_{GD2} = 0 V, t_{PULSE} < 1 µs
Continuous Drain current	I_D	20	A	T_c = 25 °C
Pulsed Drain Current (25°C, T_{Pulse} = 300 µs)	$I_{D,\ pulse}$	100	A	T_c = 25 °C
Power dissipation	P_{tot}	13	W	T_c = 25 °C
Operating temperature	T_j	-40 to +125	°C	
Storage temperature	T_{stg}	-40 to +150	°C	

2 Electrical characteristics

at T_j = 25 °C, unless specified otherwise. **Table 4 Static characteristics**

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain1-to-Drain2 Breakdown Voltage	BVD1D2S	40	-	-	V	VD2 = VG = 0 V, I_{D1D2} = 500 μA
Drain2-to-Drain1 Breakdown Voltage	BVD2D1S	40	-	-	V	VD1 = VG = 0 V, I_{D2D1} = 500 μA
Gate Threshold Voltage	$V_{GD1(TH)}$	0.8		2.4	V	V_{D1} = 0 V, V_{D2} = V_G, I_{D2D1} = 1 mA
	$V_{GD2(TH)}$	0.8		2.4		V_{D2} = 0 V, V_{D1} = V_G, I_{D1D2} = 1 mA
Zero Gate Voltage Drain Current	I_{D1D2S}	-	-	20	μA	VD2 = VG = 0 V, V_{D1} = 40 V
	I_{D2D1S}	-	-	20		VD1 = VG = 0 V, V_{D2} = 40 V
Gate-to-Drain Leakage	I_{GDS}	-		3	μA	VD1 = VD2 = 0 V, VG = 5 V
Gate-to-Drain Leakage		-30				VD1 = VD2 = 0 V, VG = -5 V
Gate-to-Drain Leakage	I_{GDS}	-		30	μA	VD1 = VD2 = 0 V, VG = 6 V
Gate-to-Drain Leakage		-40				VD1 = VD2 = 0 V, VG = -6 V
Drain1-to-Drain2 On-state Resistance	$R_{D1D2(on)}$	-	5	6	mΩ	V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C
Drain2-to-Drain1 On-state Resistance	$R_{D2D1(on)}$	-	5	6	mΩ	V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C
Gate Resistance	RG		4.1		Ω	f = 1 MHz

Table 5 Dynamic characteristics

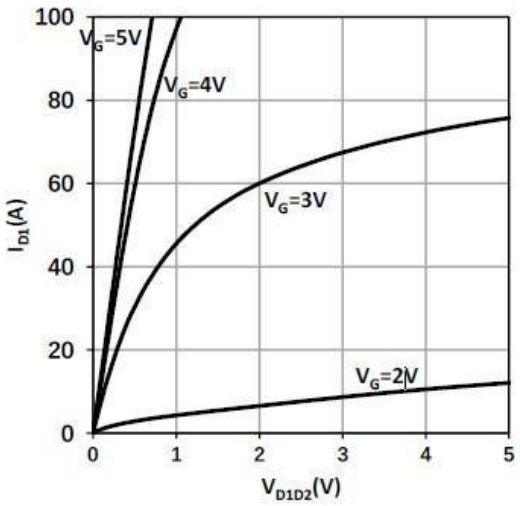
Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	900	-	pF	V_G = 0 V; V_D = 20 V; f = 100KHZ
Output capacitance	C_{oss}	-	400	-	pF	
Reverse transfer capacitance	C_{rss}	-	230	-	pF	
Total Gate Charge	Q_G	-	16	-	nC	V_D = 20 V, V_G = 5 V, ID = 10 A

Gate-to-Drain1 Charge (VD1D2=20V)	QGD1	-	1.9	-	nC	VD1 = 0, VD2 = 20 V, ID2D1 = 10 A
Gate-to-Drain1 Charge (VD1D2=20V)	QGD1		9		nC	VD2 = 0, VD1 = 20 V, ID1D2 = 10 A
Output charge	Q_{OSS}	-	12	-	nC	V_{GS} = 0 V; V_{DS} = 20 V

3 Electrical characteristics diagrams

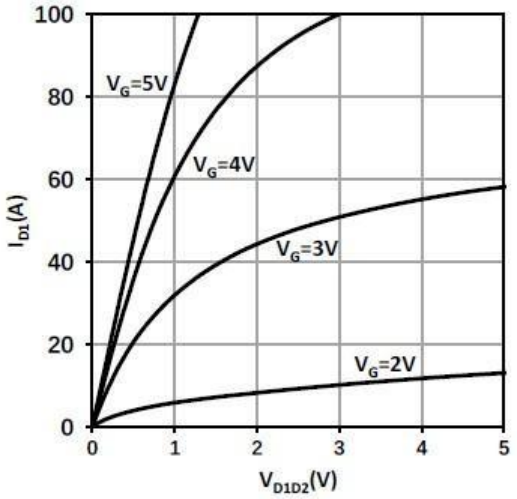
at T_j = 25 °C, unless specified otherwise.

Figure 1 Typ. output characteristics



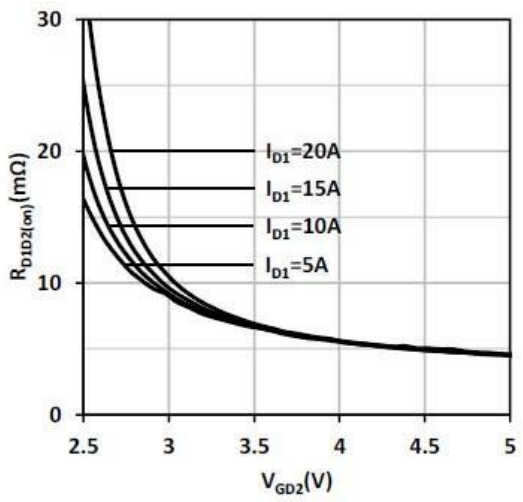
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



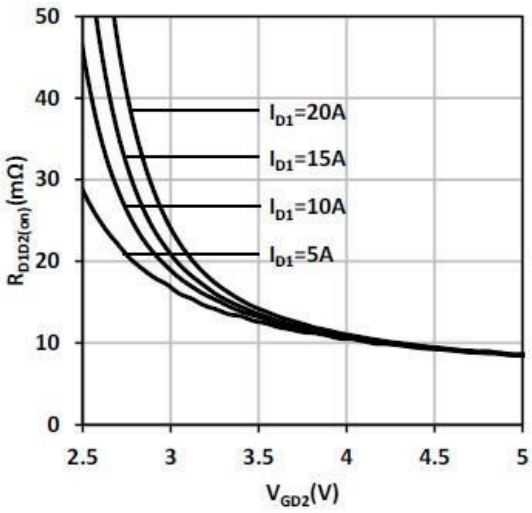
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 3 Typ. drain-source on-state resistance



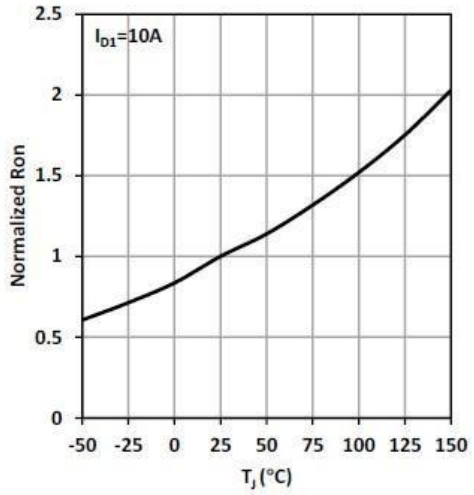
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 25 °C

Figure 4 Typ. drain-source on-state resistance



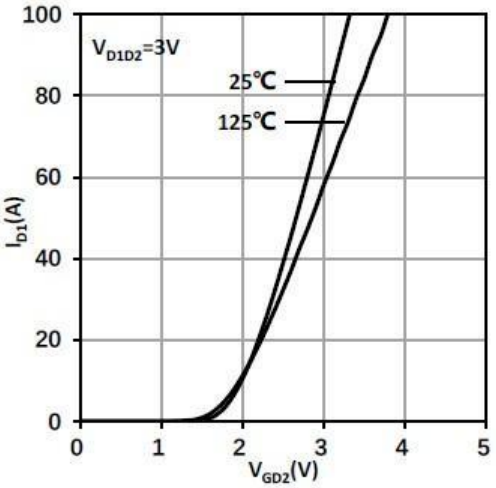
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 125 °C

Figure 5 Typ. Resistance vs. Temperature



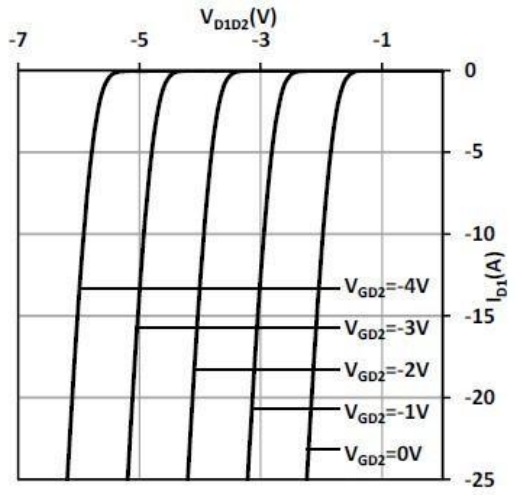
$V_{GS(TH)} = f(T_j)$; $V_{GD2} = V_{D1D2}$; I_D = 10A

Figure 6 Typ. Transfer Characteristics



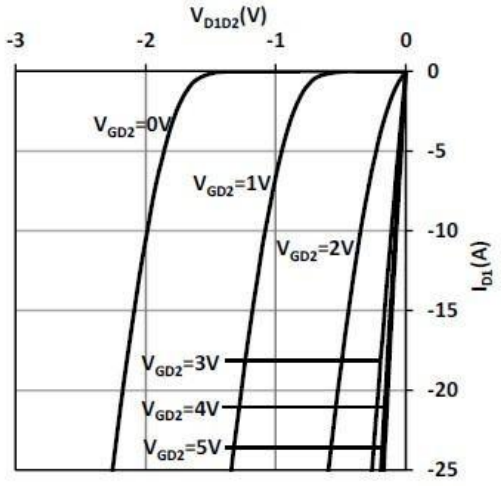
$I_D = f(V_{GD2})$; V_{D1D2} = 3V

Figure 7 Typ. Reverse Drain1-Drain2 Characteristics



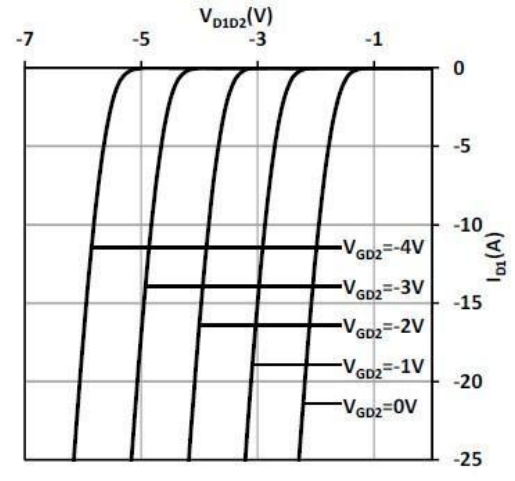
$I_D = f(V_{GD2})$; $V_{GD2} < 0$ V, $T_j = 25$ °C

Figure 8 Typ. Reverse Drain1-Drain2 Characteristics



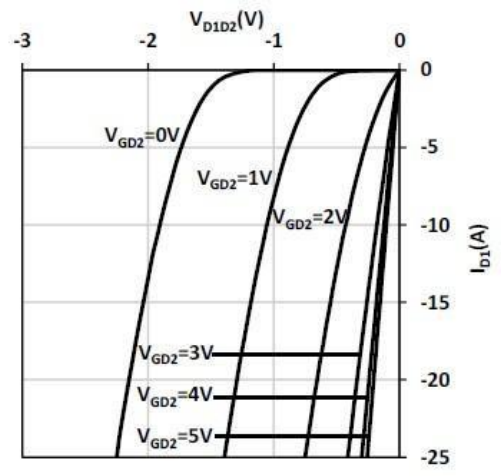
$I_D = f(V_{GD2})$; $V_{DD2} > 0$V, $T_j = 25$ °C

Figure 9 Typ. Reverse Drain1-Drain2Characteristics



$I_D = f(V_{GD2})$; $V_{GD2} < 0$ V, $T_j = 125$ °C

Figure 10 Typ. Reverse Drain1-Drain2Characteristics



$I_D = f(V_{GD2})$; $V_{GD2} < 0$ V, $T_j = 125$ °C

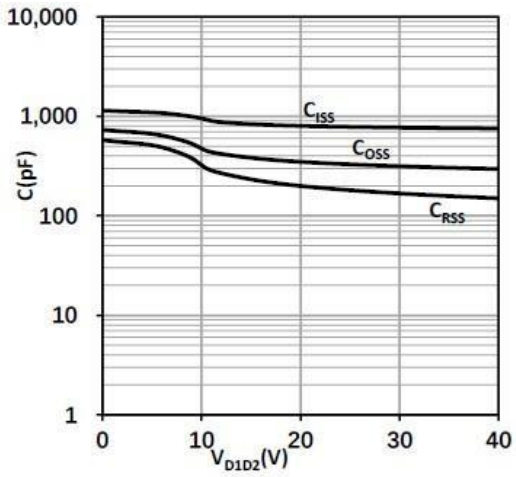
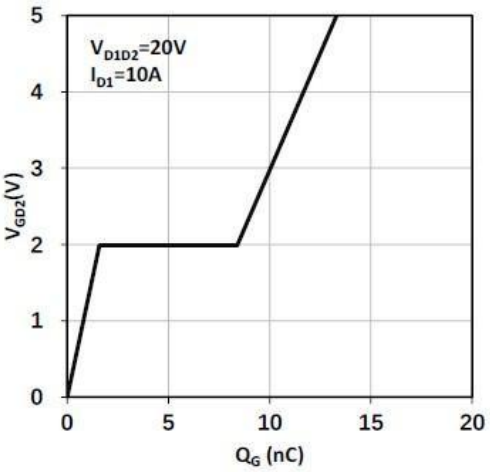
Figure 11 Typ. Capacitances Characteristics	Figure 12 Typ. Gate Charge
	
Q_{OSS} = f(V_{D1D2}); Freq. = 100khz	E_{OSS} = f(V_{D1D2}); Freq. = 100khz

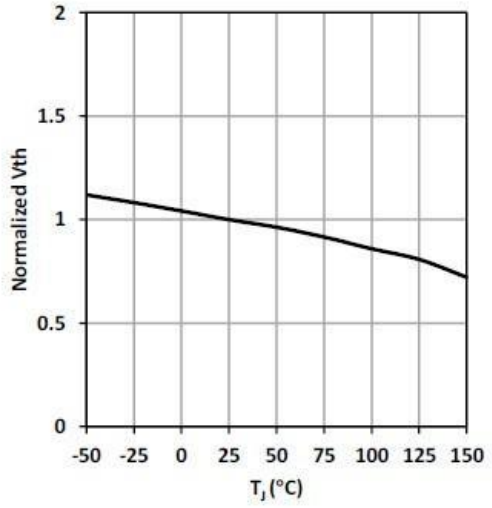
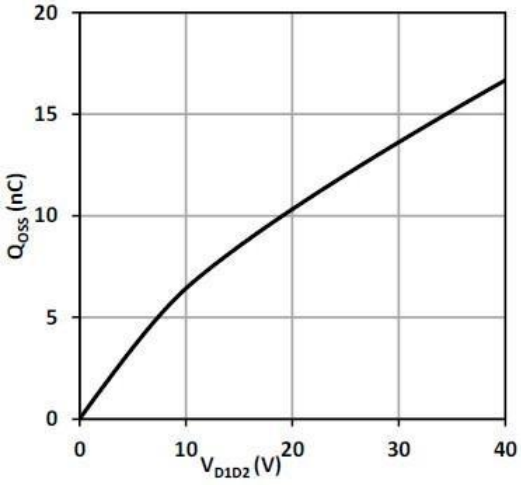
Figure 13 Normalized Threshold Voltage vs. Temp	Figure 14 Output Charge
	
$V_{GS2(TH)}$ = f(T_j); V_{GD2} = V_{D1D2}; I_D = 1 mA	Q_{OSS} = f(V_{D1D2}); Freq. = 100khz

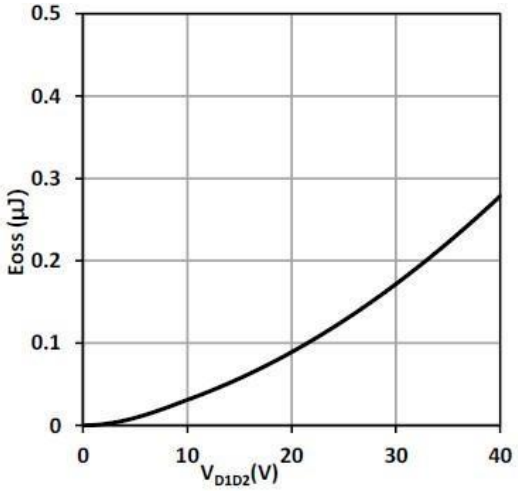
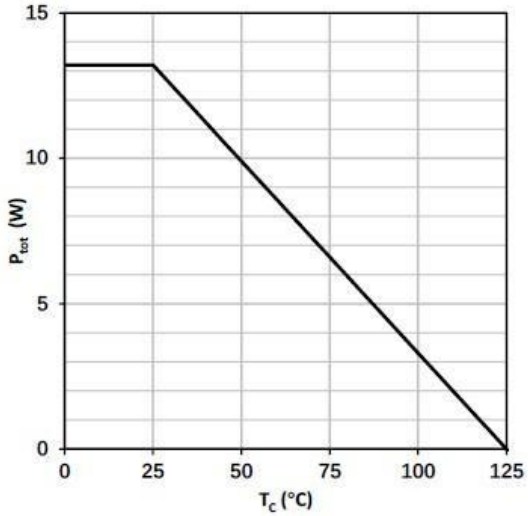
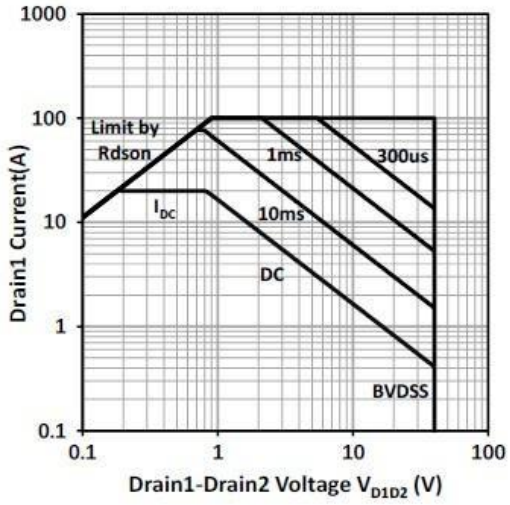
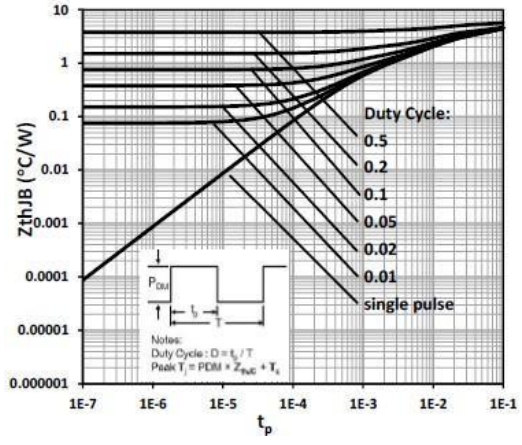
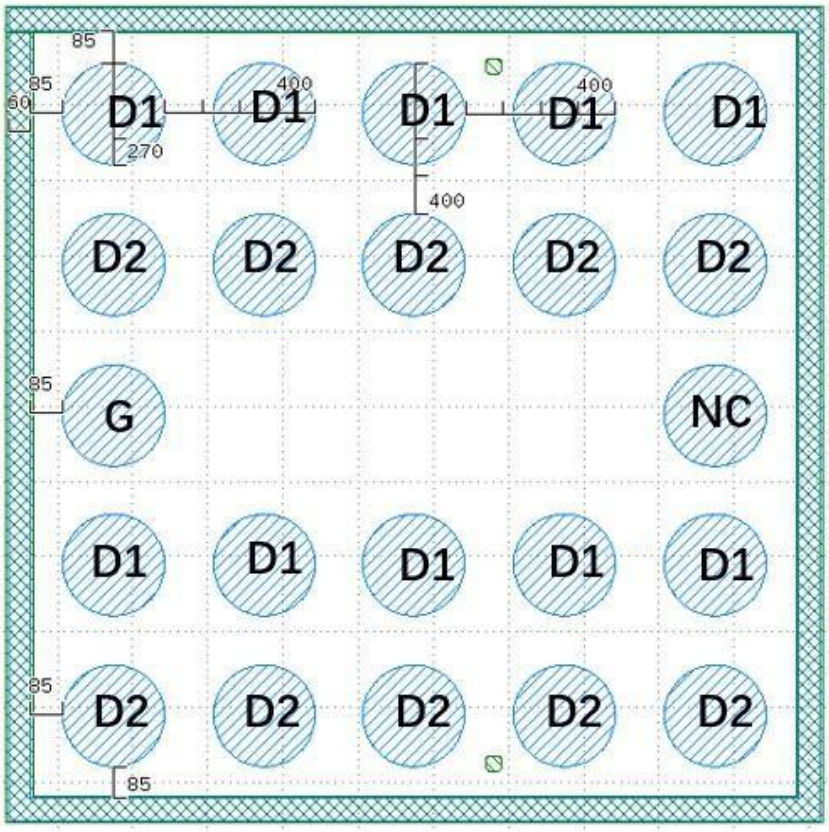
Figure 15 Output Capacitance Stored Energy	Figure 16 Power Dissipation
	
E_{OSS} = f(V_{D1D2}); Freq. = 100khz	Ptot = f(Tc)

Figure 17 Safe Operating Area	Figure 18 Max. Transient Thermal Impedance
	
Id = f(V_{D1D2}); Tc = 25℃	Zthjc = f(tp,D)

4 Package Information

Property	Parameter
Wafer Thickness	200um
Die size（With SL）	2100um*2100um
Pad diameter Size	270um
Pad pitch	400um
Top metal	4um, AlSi
Passivation	1.5 um SiO2 + 0.5um SiN



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5 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2026-04-29	1.0 initial release

6 Further Information

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