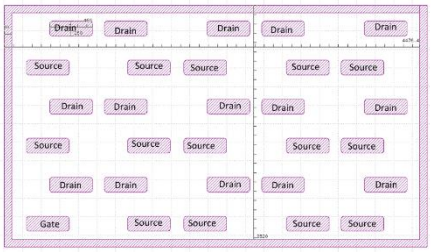
1.9mΩ 100V emode GaN



Description

This is a 100V GaN-on-Si enhancement-mode power transistor. The properties of GaN allow for high current, high breakdown voltage and high switching frequency. It is packaged in LGA or RDL suitable for low inductance high performance.

Features

- Higher switching frequency
- Lower switching losses and lower driver power
- Lower conduction
- Zero reverse recovery loss
- RoHS, Pb-free, REACH-compliant

$Q_{G,}$ typ@V_{DS}=50V	11	nC
$I_{D,\ Pulse}$	540	A
Q_{OSS} @ 50 V	56	nC

Applications

- High frequency DC-DC converter
- BMS protection
- RF envelope tracking
- PC charger
- Mobile power bank
- Motor driver

Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS,\ max}$	100	V
$R_{DS(on),\ typ}$ @V_{GS}=5V	1.9	mΩ
$R_{DS(on),\ max}$@V_{GS}=5V	2.5	mΩ

Table2 Ordering Information

Ordering Code	Type	Product code
PGLV019LG4	**LGA/RDL**	**PGLV019LG4**

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1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. **Table 3 Maximum rating**

Parameters	Symbols	Values	Units	Notes/Test Conditions
Drain-to-source voltage(Continuous)	V_{DS}	100	V	V_{GS} = 0 V
Continuous current, drain-source	I_D	275	A	T_c = 25 °C
Pulsed current, drain-source [1]	$I_{D, pulse}$	540	A	T_c = 25 °C; V_G = 5V
Pulsed current, drain-source [1]	$I_{D, pulse}$	420	A	T_c = 150 °C; V_G = 5V
Gate-source voltage, continuous	V_{GS}	-4 to +6	V	
Operating temperature	T_j	-40 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1. Pulse width = 100 µs.

2 Electrical characteristics

at T_j = 25 °C, unless specified otherwise.

Table 4 Static characteristics

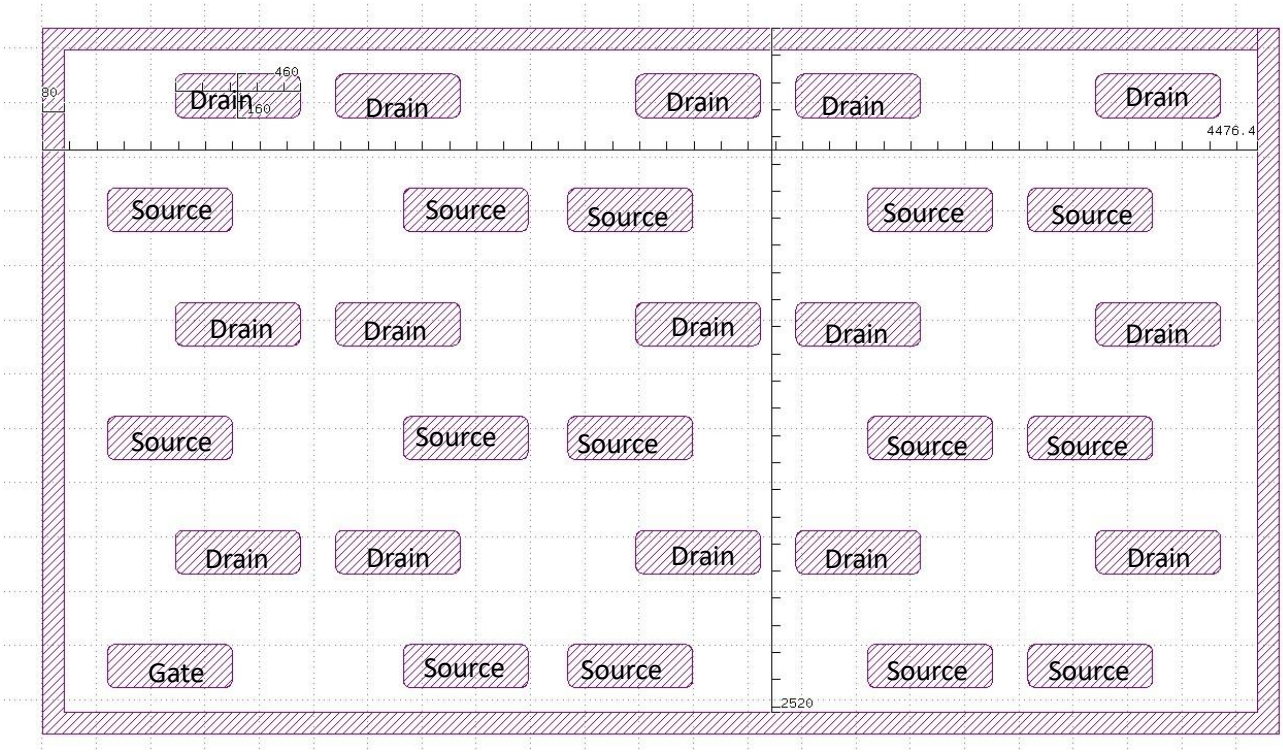
Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain to Source Voltage	BV_{DSS}	100	-	-	V	V_{GS}=0V
Gate threshold voltage	$V_{GS(TH)}$	0.8	1.1	2.5	V	I_D = 10.2 mA; V_{DS} = V_{GS}
Drain-source leakage	I_{DSS}	-	1.4	140	μA	V_{DS} = 100 V; V_{GS} = 0 V
Gate-to-source Forward leakage	I_{GSS}	-	1.4	140	μA	V_{GS} = 6 V; V_{DS} = 0 V
Gate-to-source Reverse leakage		-	0.1	140	μA	V_{GS} = -4 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.9	2.5	mΩ	V_{GS} = 5 V; I_D = 2.5 A
Source-Drain Forward Voltage	Vsd	-	1.9	-	V	I_S = 40A,V_{GS}=0V

Table 5 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1400	-	pF	V_{GS} = 0 V; V_{DS} = 50 V; f = 100KHZ
Output capacitance	C_{oss}	-	600	-	pF	V_{GS} = 0 V; V_{DS} = 50 V; f = 100KHZ
Reverse transfer capacitance	C_{rss}	-	10	-	pF	V_{GS} = 0 V; V_{DS} = 50 V; f = 100KHZ
Total Gate Charge	Q_G	-	11	-	nC	V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D= 40 A
Gate to Source Charge	Q_{GS}	-	2.6	-		V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D= 40 A
Gate to Drain Charge	Q_{GD}	-	1.7	-		V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D= 40 A
Gate Plateau Voltage	V_{Plat}	-	1.9	-	V	I_D = 40 A, V_{DS} = 50 V, V_{GS} = 0 V to 5 V
Output Charge	Q_{OSS}	-	56	-	nC	V_{GS} = 0 V, V_{DS} = 0 V to 50 V
Reverse recovery charge	Q_{RR}	-	0	-		V_{DS} = 50 V, I_S = 40 A

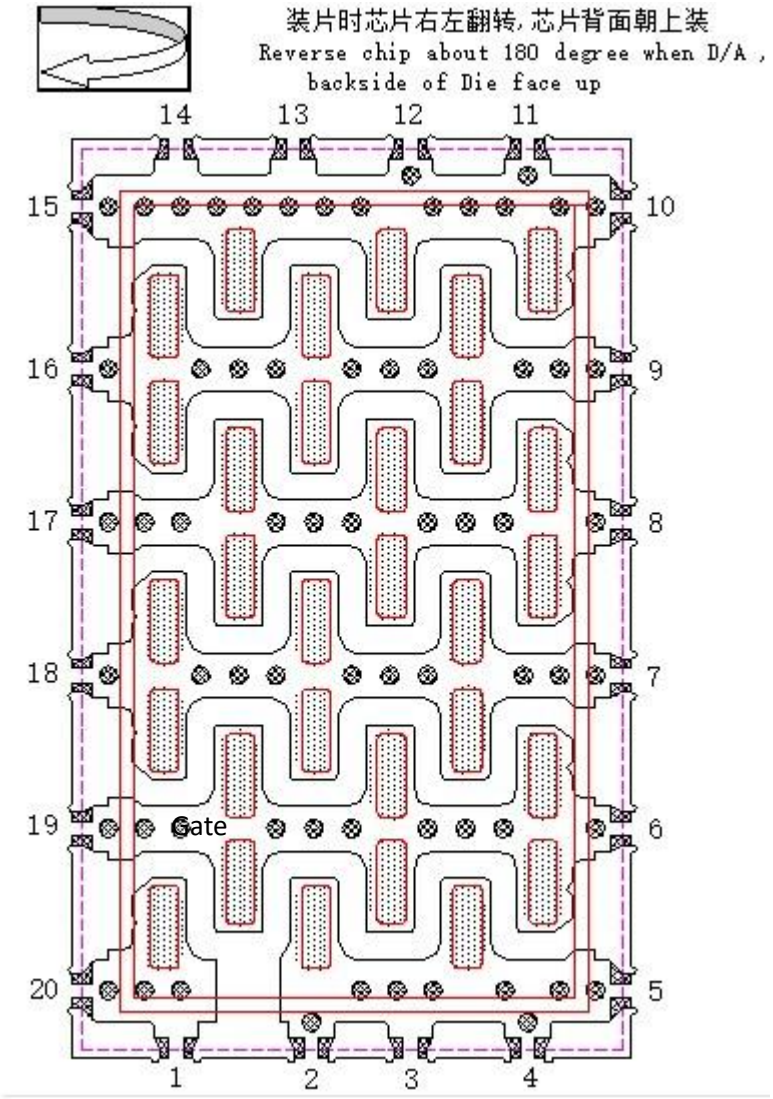
3 LGA Package Information

Parameter	Parameter
Die Thickness	200um
Die size（With SL）	4476.4um*2520um
Pad Size	460um*160um
Top metal	**ENIG**
Passivation	1.5 um SiO2 + 0.5um SiN



Notch

4 RDL Package Information



5 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2026-05-07	Initial release