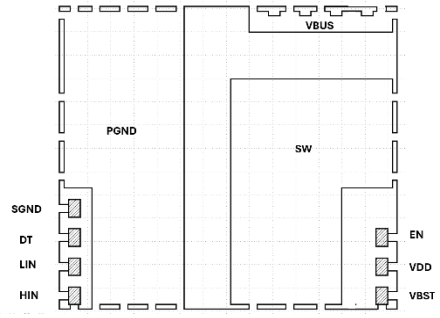
Preliminary datasheet version 1.0

Description

This is a 700V GaN-on-Si enhancement-mode power transistor packaged in half-bridge with driver IC included in the form of SiP and all-GaN-IC. The properties of GaN allow for high current, high breakdown voltage and high switching frequency. The integration of half-bridge driver makes it a high performance signal-in / power-out power stage convenient in many high power applications such as motor drivers and battery chargers. This datasheet describes the properties of driver as seen by application engineer as well as properties of a single side emode GaN HEMT.



RoHS Pb-Free HSF

Table 1 Key Performance Parameters of main emode GaN at T_j = 25 °C

Parameters	Values	Units
$V_{DS, max}$	700	V
$R_{DS(on), typ}$	47	mΩ
Q_G	11	nC
$I_{D, Pulse}$	60	A
Q_{OSS} @ 400 V	160	nC
Q_{rr}	0	nC

Features

- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection
- UVLO Protections for VDD High and Low−Side Drivers
- 200 V/ns dV/dt Rating for all SW and PGND Referenced Circuitry
- Maximum Propagation Delay of Less Than 50 ns
- Matched Propagation Delays to Less Than 5 ns
- User Programmable Dead−Time Control
- Thermal Shutdown (TSD)
- RoHS, Pb-free, REACH-compliant

Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast Battery charging
- Efficient and smooth motor drive
- High density power conversion
- High efficiency power conversion

Table2 Ordering Information

Ordering Code	Package	Product code
GP70R47HBIC15	**Half-Bridge QFN**	**GP70R47HBIC15**

Table of contents

1 Maximum ratings for emode GaN switch

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime.

Table 3 Maximum rating

Parameters	Symbols	Values	Units	Notes/Test Conditions
Drain-source voltage	$V_{DS, max}$	700	V	V_{GS} = 0 V Tj = -55℃ to 150℃
Drain-source voltage transient [1]	$V_{DS, transient}$	800	V	V_{GS} = 0 V
Continuous current, drain-source	I_D	40	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	60	A	T_c = 25 °C; V_G = 6 V
Pulsed current, drain-source [2]	$I_{D, pulse}$	30	A	T_c = 125 °C; V_G = 6 V
Gate-source voltage, continuous	V_{GS}	-6 to +6	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-20 to +10	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	**300**	W	T_c = 25 °C
Operating temperature	T_j	-55 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 µs.
2. Pulse width = 10 µs.

2 Electrical characteristics of emode GaN switch

at T_j = 25 °C, unless specified otherwise.

Table 4 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.0	1.6	2.5	V	I_D = 32 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	2	-		I_D = 32mA; V_{DS} = V_{GS}; T_j = 150 °C
Drain-source leakage current	I_{DSS}	-	0.1	3.2	μA	V_{DS} = 700 V; V_{GS} = 0 V; T_j = 25 °C
		-	2	-		V_{DS} = 700 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	11		μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state Resistance[1]	$R_{DS(on)}$	-	47	55	mΩ	V_{GS} = 6 V; I_D = 2 A; T_j = 25 °C
		-	90	-	mΩ	V_{GS} = 6 V; I_D = 2A; T_j = 150 °C
Gate resistance	R_G	-	4	-	Ω	f = 5 MHz; open drain

4 Driving control pin description

Pin name	Description
DT	Dead time adjustment
SGND	Signal ground
LIN	Logic input for low side driving
HIN	Logic input for high side driving
EN	Logical input for enable/disable of the driving system
VDD	Bias voltage for high current driver
VBST	Bootstrap positive bias voltage

5 Driver absolution maximum ratings

All voltages are referenced to SGND pin unless otherwise noted.

Symbol	Rating	Min	Max	Unit
VDD	Low−side and logic−fixed supply voltage (PGND = SGND)	-0.3	20	V
VBST	High−side floating supply voltage VBST	-0.3	670	V
VIN	LIN, HIN, EN Logic input voltage	-0.3	VDD+0.3	V
VDT	Dead−time control voltage (DT)	-0.3	VDD+0.3	V
TJ	Operating Junction Temperature		150	C
TSTG	Storage Temperature Range	-55	150	C
ESD	HBM/CDM		1	kV

6 Recommended Driver Operating Condition

Symbol	Rating	Min	Max	Unit
VDD	**Low−side and logic−fixed supply voltage**	**9**	**17**	**V**
VSW	**SW−SGND maximum dc offset voltage (High−Side driver)**		**580**	**V**
VBST	**High−side floating supply voltage VBST**		**VSW+17**	
VIN	**Logic input voltage (HIN, LIN, and EN)**		**17**	**V**

7 Driver Electrical Characteristics

Conditions: (VBIAS (VDD, VBST) = 15 V, DT = SGND = PGND and CLOAD = 330 pF for typical values TJ = 25°C, for min/max values TJ = −40°C to +125°C, unless otherwise specified.) The VIN and IIN parameters are referenced to SGND.

Min/Typical/Max Values

POWER SUPPLY SECTION (VDD)

IQDD	VDD Quiescent current	VIN=0		100	150	μA
IPDD	VDD operating currnt	fLIN=500kHz		1.5	2.5	mA
VDDUV+	VDD UVLO + threshold	VDD=sweep	8.0	8.5	9.0	V
VDDUV-	VDD UVLO- threshold	VDD=sweep	7.5	8.0	8.5	V
VDDHYS	**VDD UVLO Hysteresis**	**VDD = Sweep**		0.5		V
tUVDDFLT	**VDD UVLO Filter Delay Time**			5.3		μS

BOOTSTRAPPED POWER SUPPLY SECTION

ILK	**Offset supply leakage current**	**VBST = VSW = 600 V**			**10**	**μA**
IQBST	**Quiescent VBST supply current**	**VLIN = VHIN = 0 V, EN = 5 V**		**35**	**100**	**μA**
IPBST	**Operating VBST supply current**	**HIN = 500 kHz, average value**		**1.5**	**2.5**	**mA**
VBSTUV+	**VBST UVLO positive going threshold**	**VDD = 12 V**	**6**	**6.5**	**7**	**V**
VBSTUV−	**VBST UVLO negative going threshold**	**VDD = 12 V**	**5.5**	**6**	**6.5**	**V**
VHYST	**VBST UVLO Hysteresis**	**VDD = 12 V**		**0.5**		**V**

INPUT LOGIC SECTION (HIN, LIN and EN)

VINH	**High Level Input Voltage Threshold**				2.5	V
VINL	**Low Level Input Voltage Threshold**		1.2			V
VIN_HYS	**Input Logic Voltage Hysteresis**			0.5		V
IIN+	**High Level Logic Input Bias Current**	**VHIN = VLIN = 5 V**	9	15	21	μA
IIN−	**Low Level Logic Input Bias Current**	**VHIN = VLIN = 0 V**			2.2	μA
RIN	**Input Pull−down Resistance**	**VHIN = VLIN = 5 V**		333		kΩ

DEAD−TIME SECTION

VDT,MIN	**Minimum Dead−Time Control Voltage**	**RDT = 30 kΩ**	0.45	0.60	0.75	V
tDT,MIN			22	30	38	nS
VDT,MAX	**Maximum Dead−Time Control Voltage**	**RDT = 200 kΩ**	3.1	4.0	4.8	V
tDT,MAX			160	200	240	nS
ΔtDT	**Dead−Time mismatch between LO → HO and HO →LO**	**RDT = 30 kΩ**			5	nS
		RDT = 200 kΩ			10	nS
VDT,0	**Dead−Time Disable Threshold**	**Cross conduction prevention active**	0.35	0.4	0.45	V
VDT,OLE	**High− & Low−Side Overlap Enable Threshold**	**Cross conduction prevention disabled**	5.5	6.0	6.5	V

PROTECTION SECTION

VUVTH_VDDX+	**UVLO Threshold on VDDH and VDDL positive going threshold**		**4.15**	4.4	4.7	V
VUVTH_VDDX−	**UVLO Threshold on VDDH and VDDL negative going threshold**		**4.0**	4.2	4.5	V
TSD	**Thermal Shutdown**		150			C
hys	**Hysteresis of Thermal Shutdown**			50		C

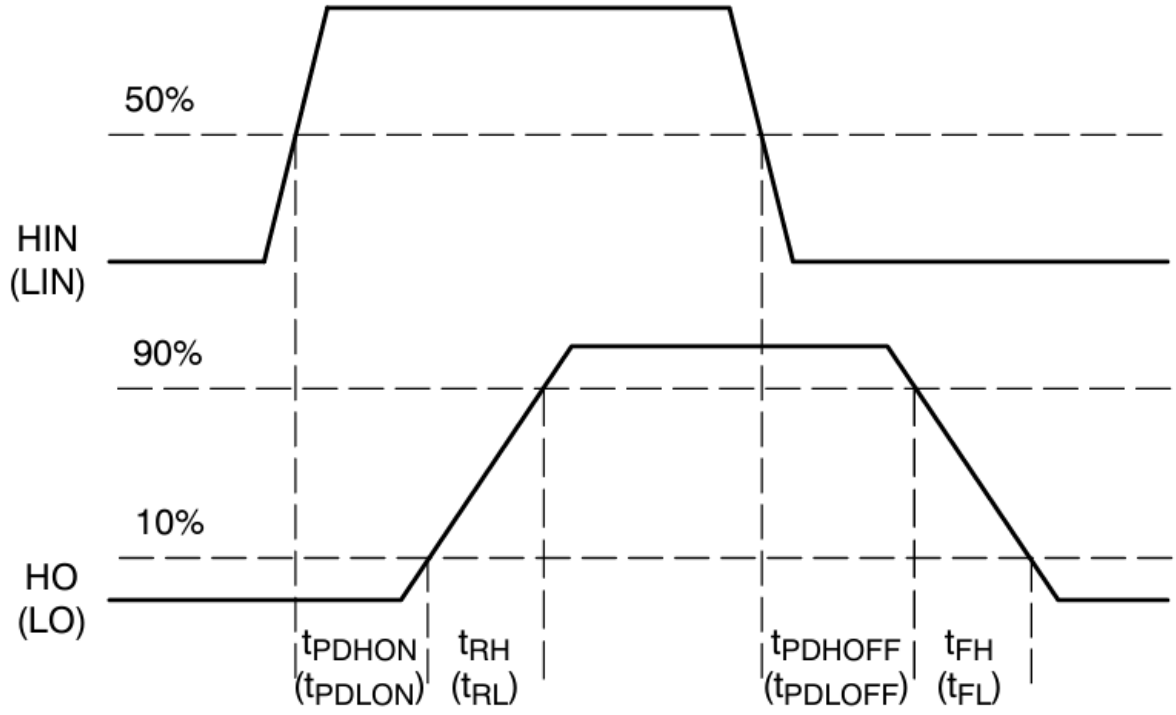
8 Driver Dynamic Characteristics

Conditions: (VBIAS (VDD, VBST)=15 V, DT=SGND=PGND and CLOAD=330 pF, for typical values TA=25°C, for min/max values TA=−40°C to +125°C, unless otherwise specified.)

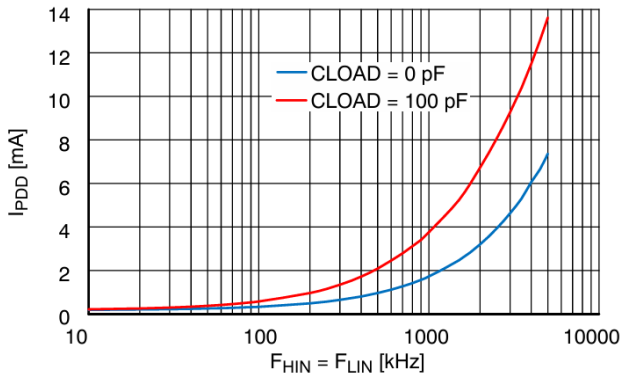
IQDD	**Quiescent VDD supply current**	**VLIN = VHIN = 0 V, EN = 0 V**		**100**	150	μA

tPDLON	**LOSRC turn−on propagation delay time**	**LIN rising to LOSRC rising (50% to 10%)**		25	50	nS
tPDLOFF	**LOSNK turn−off propagation delay time**	**LIN falling to LOSNK falling (50% to 90%)**		**25**	50	nS
tPDHON	**HOSRC turn−on propagation delay time**	**HIN rising to HOSRC rising (50% to 10%) SW = PGND**		**25**	50	nS
tPDHOFF	**HOSNK turn−off propagation delay time**	**HIN falling to HOSNK falling (50% to 90%) SW = PGND**		**25**	50	nS
tRL	**LOSRC turn−on rising time**			**2**	4	nS
tFL	**LOSNK turn−off falling time**			**1.5**	3.0	nS
tRH	**HOSRC turn−on rising time**	**SW = PGND**		**2**	4	nS
tFH	**HOSNK turn−off falling time**	**SW = PGND**		**1.5**	3.0	nS
∆tDEL	**Propagation Delay match**	**HIN to HO and LIN to LO, SW = PGND**			5	nS
tPW	**Minimum input pulse width**				10nS	nS

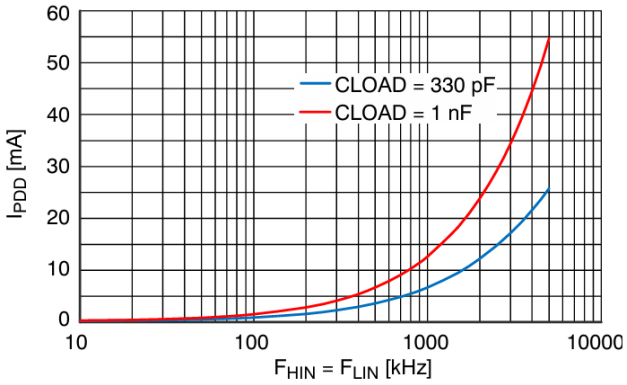
TIMING DIAGRAM



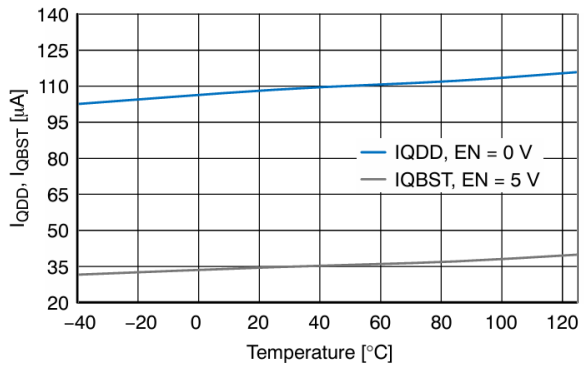
9 Driver Data Figures



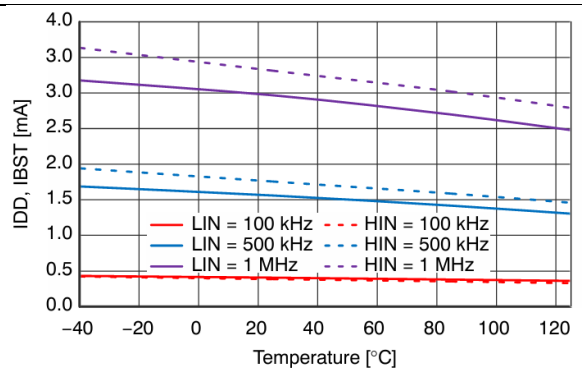
Operating VDD Supply Current (IPDD) vs. Frequency (VDD = 12 V, SW = PGND, EN = VDD, Both Outputs Switching)



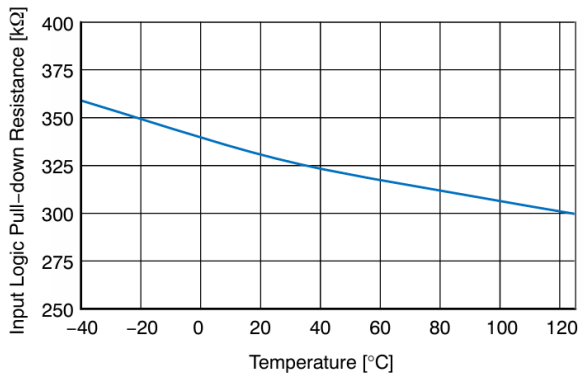
Operating VDD Supply Current (IPDD) vs. Frequency (VDD = 12 V, SW = PGND, EN = VDD, Both Outputs Switching)



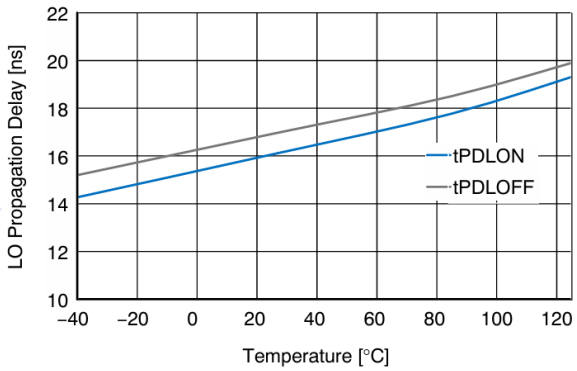
Quiescent Current (IQDD, IQBST) vs. Temperature



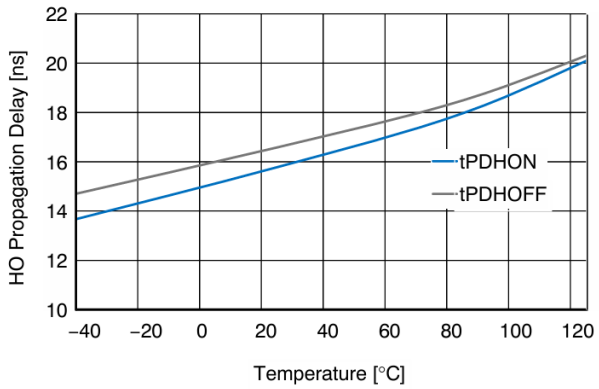
Operating Current (IPDD, IPBST) vs. Temperature



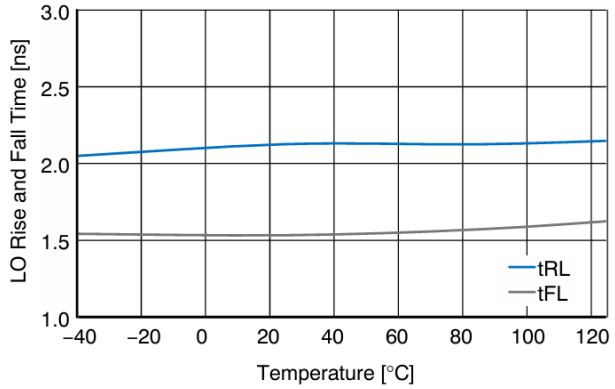
Input Logic (HIN, LIN, EN) Pull−down Resistance vs. Temperature



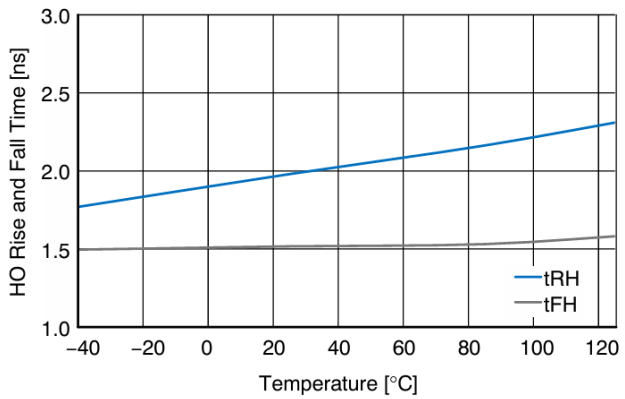
LIN to LOSRC Propagation Delay vs. Temperature



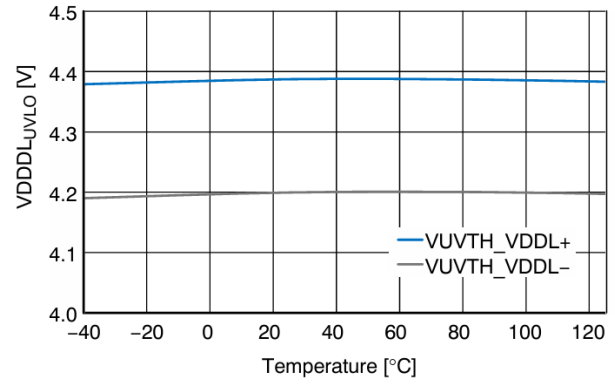
HIN to HOSRC Propagation Delay vs. Temperature



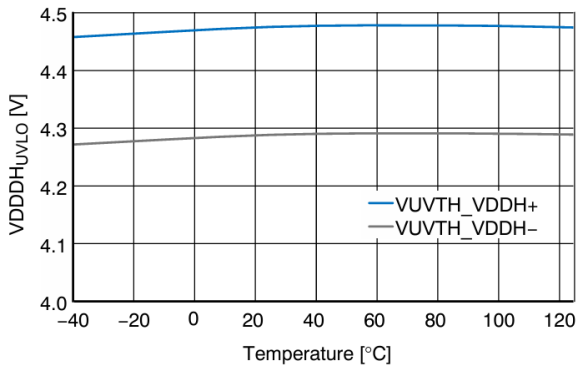
LOSRC Rise Time and LOSNK Fall Time vs. Temperature



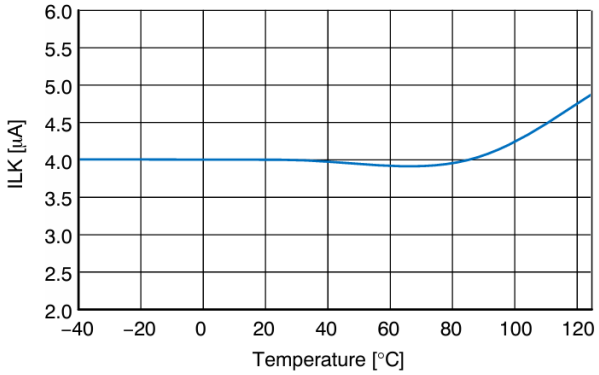
HOSRC Rise Time and HOSNK Fall Time vs. Temperature



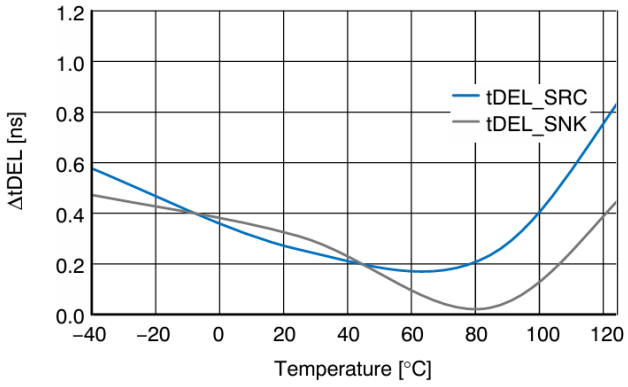
VDDL UVLO vs. Temperature



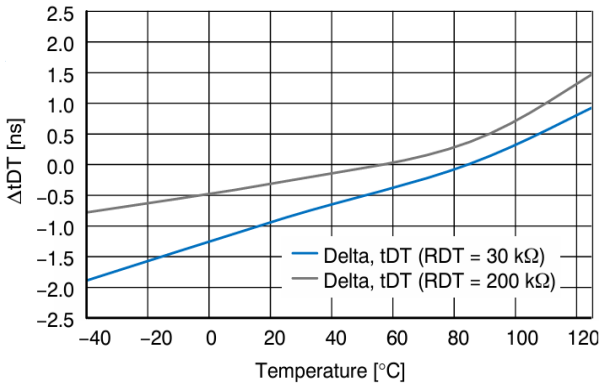
VDDH UVLO vs. Temperature



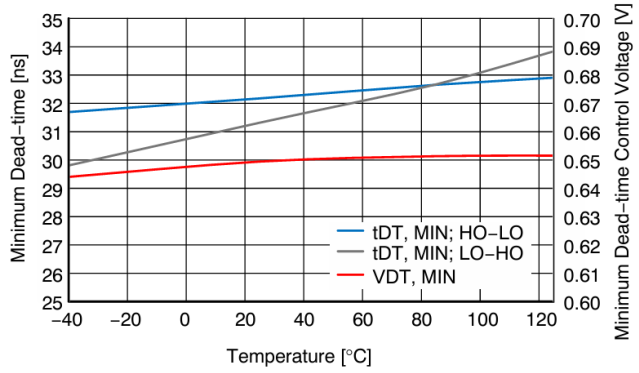
VBST Leakage Current (ILK) vs. Temperature



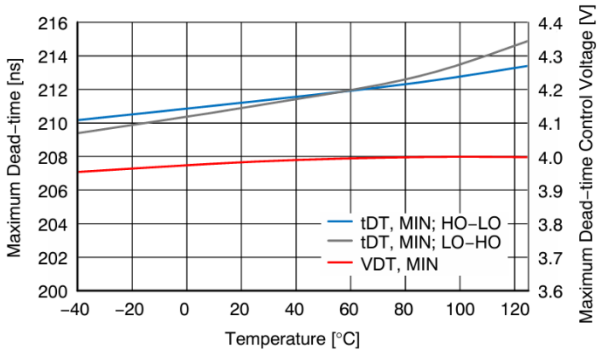
Propagation Delay Matching (HIN to HO, LIN to LO) vs. Temperature



Dead−time Mismatch vs. Temperature



Minimum Dead−time (RDT = 30 k) vs. Temperature



Maximum Dead−time (RDT = 200 k) vs. Temperature

10 Application Information

The following circuit configuration is recommended.

Depending on different switching frequencies, different sets of matching passive components shall be used as follows:

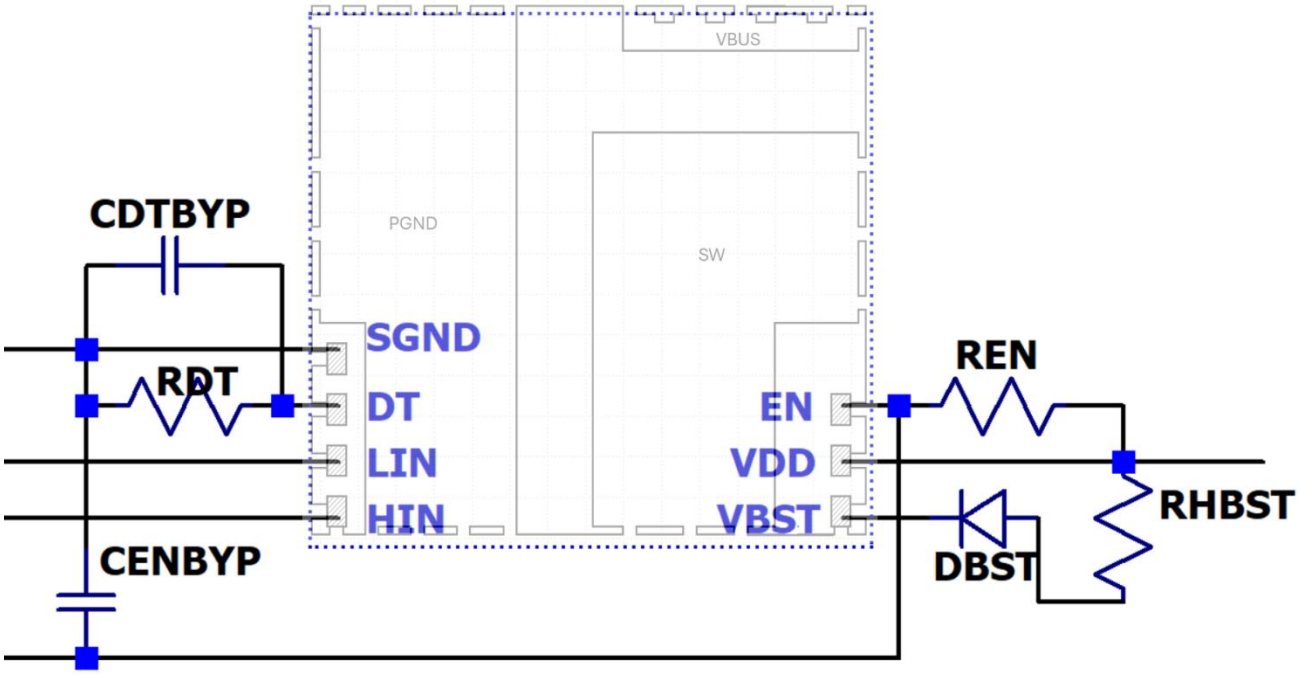


Table A: Application #1 – Motor Drive (10-30kHz)

Designator	Value	Description	Package
REN	10 kΩ	Enable pull-up resistor (to VDD)	0402
CENBYP	100 pF / 50V	Enable pin noise filter	0402
CDTBYP	100 nF / 16V	DT pin noise bypass capacitor (X7R)	0201 or 0402
RDT	56kΩ	Programs ~40-50ns dead-time	0402
RBST	10 Ω	Bootstrap current limit	0402
DBST	ES1J (or ES1D)	600V, 1A Ultrafast recovery diode	SMA / DO-214AC

Table B: Application #2 – PFC Stage (100-150kHz)

Designator	Value	Description	Package
REN	10 kΩ	Enable pull-up resistor (to VDD)	0402
CENBYP	10 pF / 50V	Minimal filtering for fast enable response (NP0)	0402
CDTBYP	100 nF / 16V	DT pin noise bypass capacitor (X7R)	0201 or 0402
RDT	27 kΩ	Programs ~25-30ns dead-time	0402
RBST	2.2 Ω	Low resistance for fast CVBST recharge	0402
DBST	BAS21 (or BAV21)	250V, 200mA, Ultra-low capacitance (2pF)	SOD-123

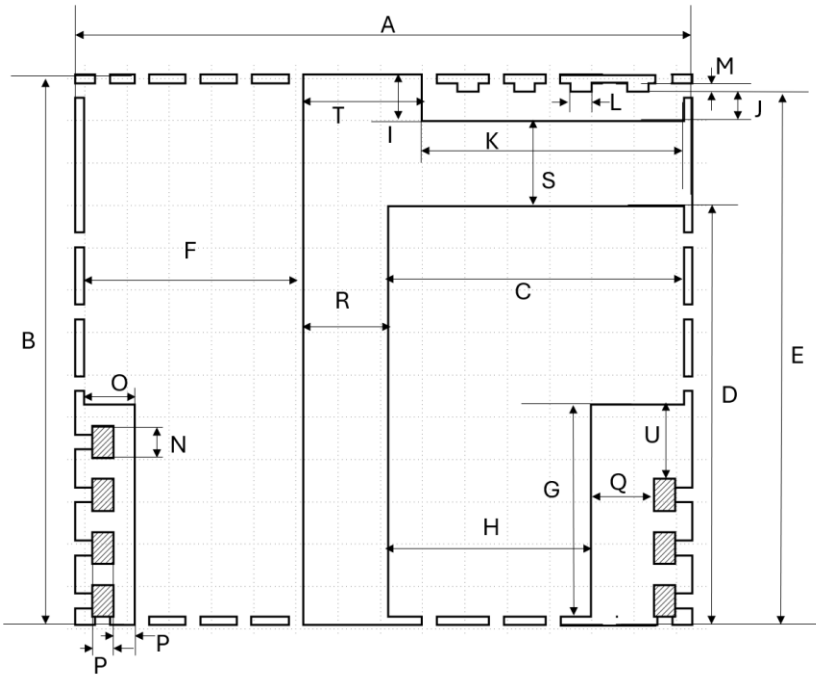
Table C: Application #3 – LLC DC-DC (300kHz)

Designator	Value	Description	Package
REN	10 kΩ	Enable pull-up resistor (to VDD)	0402
CENBYP	10 pF / 50V	High-frequency noise bypass (NP0)	0402

Designator	Value	Description	Package
CDTBYP	100 nF / 16V	DT pin noise bypass capacitor (X7R)	0201 or 0402
RDT	18kΩ	Programs ~15-20ns dead-time	0402
RBST	0 Ω (Jumper)	Minimize impedance for fastest recharge	0402
DBST	SD103AWS	40V, 350mA, Schottky (No reverse recovery)	SOD-123

11 Package Information

This product is packaged in QFN15x13 with the following POD/leads in top view:



	mm		mm
A	14.6	L	0.5
B	13	M	0.2
C	7	N	0.75
D	9.7	O	1.2
E	12.6	P	0.5
F	5.2	Q	1.5
G	5	R	2
H	4.8	S	2
I	1.1	T	2.8
J	0.7	U	1.76
K	6.2	SMD THICK	3.0

12 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.1	2026-04-29	1.0 version release

13 Further Information

Important Notice-Unless expressly approved in writing by an authorized representative of GaNPower, GaNPower components are not designed, authorized or warranted for use in lifesaving, life sustaining, military, aircraft, or space applications, nor in products or systems where failure or malfunction may result in personal injury, death, or property or environmental damage. The information given in this document shall not in any event be regarded as a guarantee of performance. GaNPower hereby disclaims any or all warranties and liabilities of any kind, including but not limited to warranties of non-infringement of intellectual property rights. All other brand and product names are trademarks or registered trademarks of their respective owners. Information provided herein is intended as a guide only and is subject to change without notice. The information contained herein or any use of such information does not grant, explicitly, or implicitly, to any party any patent rights, licenses, or any other intellectual property rights.

Data Source– Data here are based on recent tests but all parameters may not be up to date. Actual final test data from packaging production are available for selected customers upon request.