GP70R140T2P N-MOS Compatible 700V 140 mΩ GaN Power HEMT

700V/140mΩ **Preliminary Datasheet V1.0**

Description

This is a 700V GaN-on-Si enhancement-mode power transistor. The properties of GaN allow for high current, high breakdown voltage and high switching frequency.

Features

- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection
- RoHS, Pb-free, REACH-compliant

$I_{D,\text{ Pulse}}$	20.5	A
Q_{OSS} @ 400 V	24	nC
Q_{rr}	0	nC

Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS,\text{ max}}$	700	V
$R_{DS(on),\text{ Typ}}$	140	mΩ
Q_G	2.8	nC

Applications

- AC/DC converters
- DC/DC converters
- Bridgeless totem pole PFC
- Fast chargers
- Power adapters
- LED lighting drivers
- Wireless power transfer
- Laser drivers • TV display

Table2 Ordering Information

Ordering Code	Package	Product code
GP70R140T2P	TO220FP	GP70R140T2P

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1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime.

Table 3 Maximum rating

Parameters	Symbols	Values	Units	Notes/Test Conditions
Drain-source voltage	$V_{DS,\ max}$	700	V	V_{GS} = 0 V Tj = -55℃ to 150℃
Drain-source voltage transient [1]	$V_{DS,\ transient}$	800	V	V_{GS} = 0 V
Continuous current, drain-source	I_D	11.5	A	T_c = 25 °C

Pulsed current, drain-source [2]	$I_{D,\ pulse}$	20.5	A	T_c = 25 °C; V_G = 6 V
Pulsed current, drain-source [2]	$I_{D,\ pulse}$	11.5	A	T_c = 125 °C; V_G = 6 V
Gate-source voltage, continuous	V_{GS}	-6 to +20	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS,\ pulse}$	-20 to +20	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	83	W	T_c = 25 °C
Operating temperature	T_j	-55 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1. $V_{DS,\ transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 µs.

2. Pulse width = 10 µs.

2 Electrical characteristics

at T_j = 25 °C, unless specified otherwise.

Table 4 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	2.0	2.6	3.5	V	I_D = 11.4 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	3	-		I_D = 11.4 mA; V_{DS} = V_{GS}; T_j = 150 °C
Drain-source leakage current	I_{DSS}	-	0.03	1.1	µA	V_{DS} = 700 V; V_{GS} = 0 V; T_j = 25 °C
		-	1.5	-		V_{DS} = 700 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	4		mA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state Resistance[1]	$R_{DS(on)}$	-	140	170	mΩ	V_{GS} = 6 V; I_D = 3.9 A; T_j = 25 °C
		-	320	-	mΩ	V_{GS} = 6 V; I_D = 3.9 A; T_j = 150 °C
Gate resistance	R_G	-	6.5	-	Ω	f = 5 MHz; open drain

1. $R_{DS(on)}$ is the test of fresh devices

Table 5 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	82	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100KHZ
Output capacitance	C_{oss}	-	35	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100KHZ
Reverse transfer capacitance	C_{rss}	-	0.53	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100KHZ
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	45	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	60	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	24	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	1.4	-	ns	V_{DS} = 400 V; I_D = 8 A; L = 318 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω
Turn-off delay time	$t_{d(off)}$	-	1.7	-	ns	
Rise time	t_r	-	4	-	ns	
Fall time	t_f	-	4	-	ns	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 6 Gate charge characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	2.8	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 3.9 A
Gate-source charge	Q_{GS}	-	0.25	-	nC	
Gate-drain charge	Q_{GD}	-	1.1	-	nC	
Gate plateau voltage	V_{plat}	-	2.5	-	V	V_{DS} = 400 V; I_D = 3.9 A

Table 7 Reverse conduction characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	3.8	-	V	V_{GS} = 0 V; I_{SD} = 3.9 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	-	20.5	A	V_{GS} = 6 V

Reverse recovery charge [1]	Q_{rr}	-	0	-	nC	I_{SD} = 3.9 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

[1] Excluding Q_{OSS}

3 Electrical characteristics diagrams

at T_j = 25 °C, unless specified otherwise.

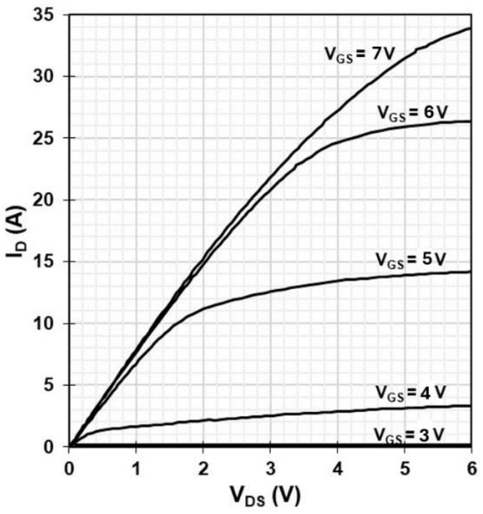
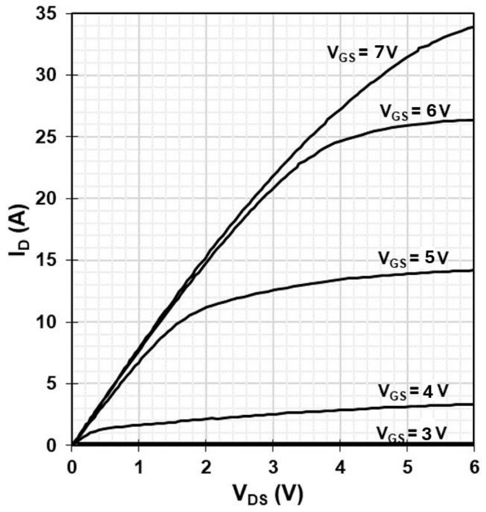
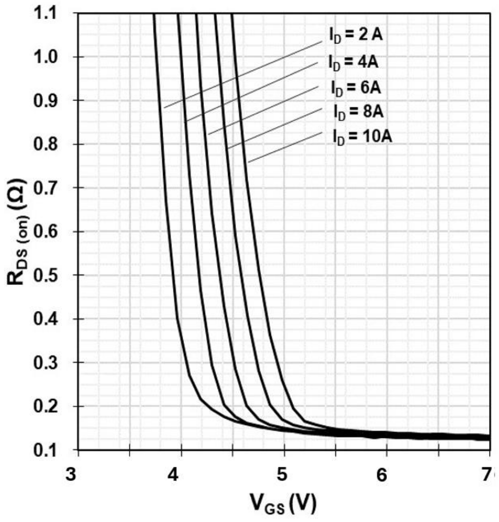
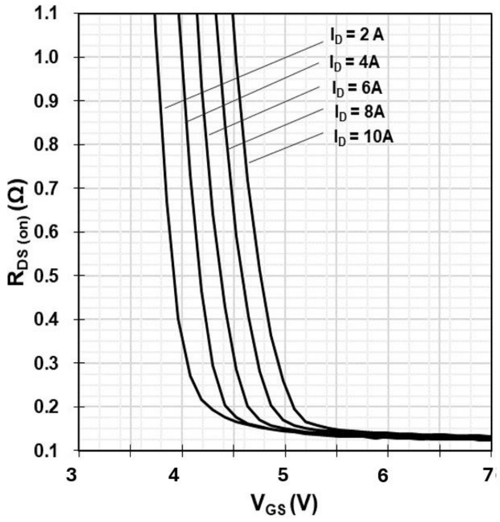
Figure 1 Typ. output characteristics	**Figure 2 Typ. output characteristics**
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 3 Typ. drain-source on-state resistance



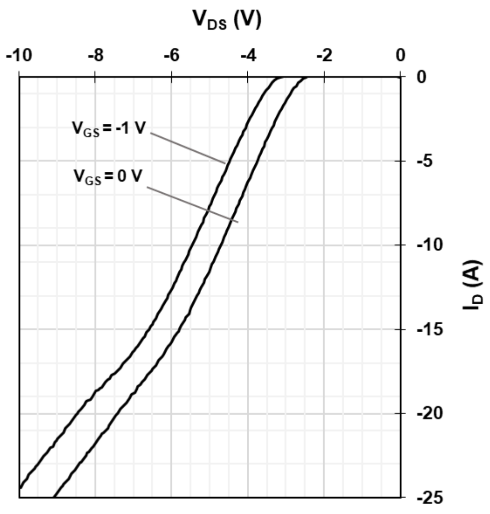
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 25 $_o$C

Figure 4 Typ. drain-source on-state resistance



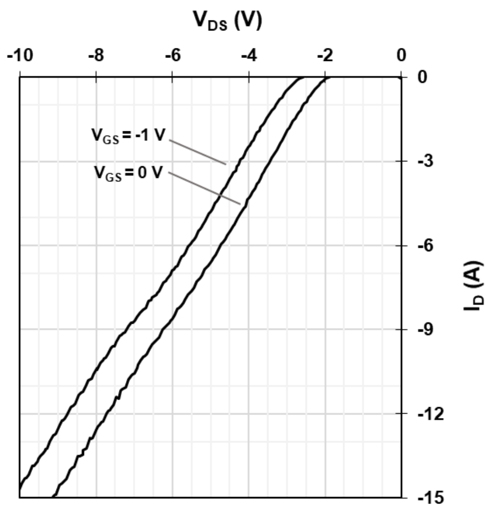
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 125 $_o$C

Figure 5 Typ. channel reverse characteristics



$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 6 Typ. channel reverse characteristics



$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

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Figure 7 Typ. channel reverse characteristics

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Figure 8 Typ. channel reverse characteristics

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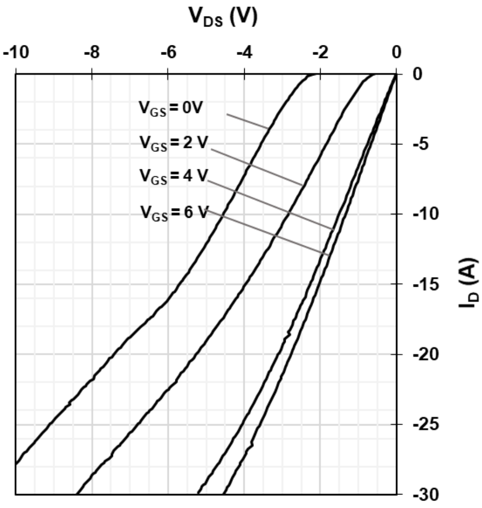

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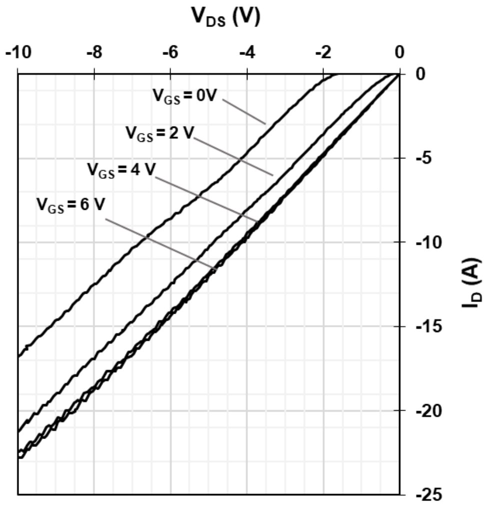

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$I_D = f(V_{DS}, V_{GS})$; $T_j = 25$ °C

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$I_D = f(V_{DS}, V_{GS})$; $T_j = 125$ °C

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Figure 9 Typ. transfer characteristics

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Figure 10 Typ. gate-to-source leakage

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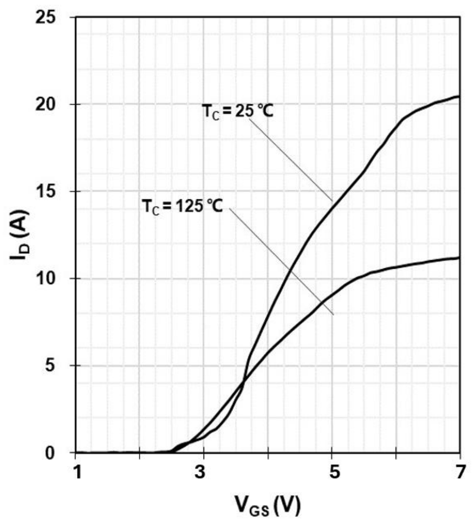

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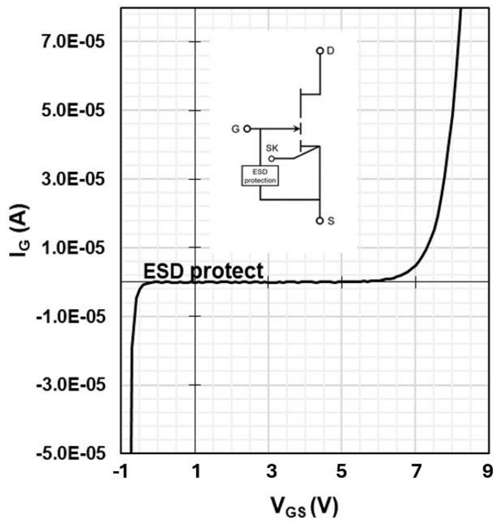

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$I_D = f(V_{GS})$; $V_{DS} = 3$ V

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$I_G = f(V_{GS})$; V_D = open

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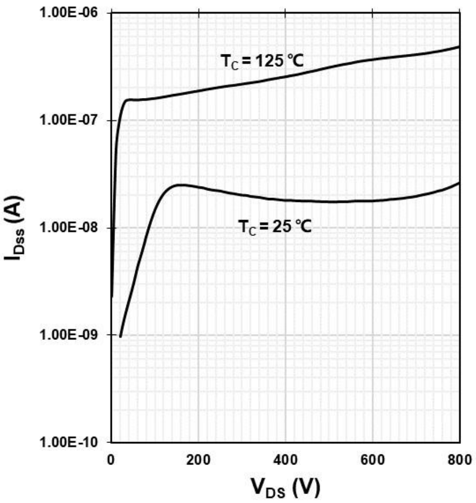
Figure 11 Drain-source leakage characteristics

Idss = f(Vds); Vgs = 0V

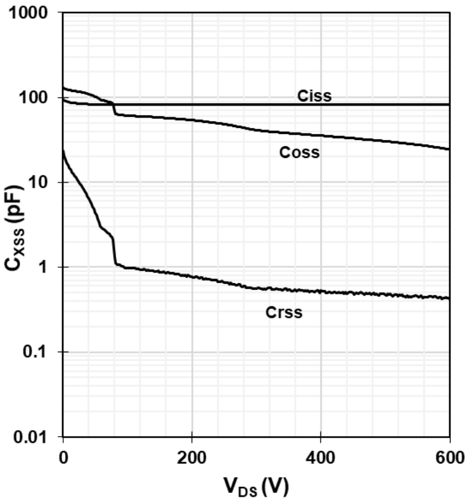
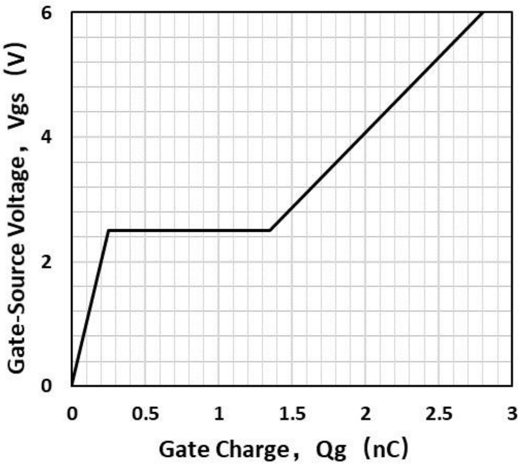
Figure 12 Typ. capacitances	**Figure 13 Typ. gate charge**
	
C_{XSS} = f(V_{DS}); Freq. = 100kHz	V_{GS} = f(Q_G); V_{DS} = 400 V; I_D = 3.9 A

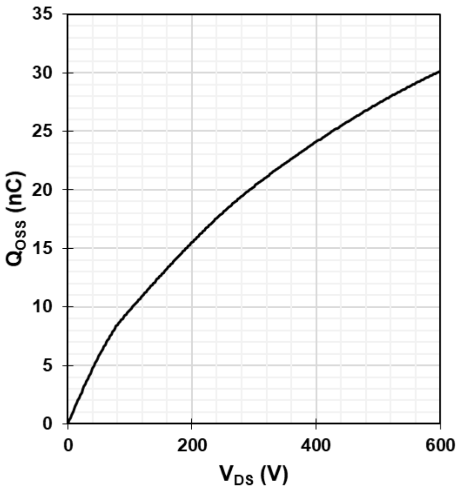
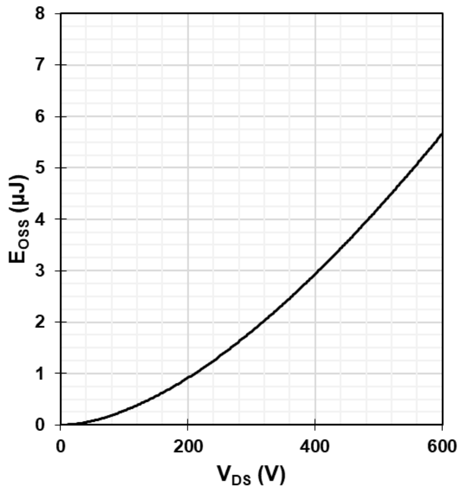
Figure 14 Typ. output charge	**Figure 15 Typ. C_{OSS} stored energy**
	
$Q_{OSS} = f(V_{DS})$; Freq. = 100khz	$E_{OSS} = f(V_{DS})$; Freq. = 100khz

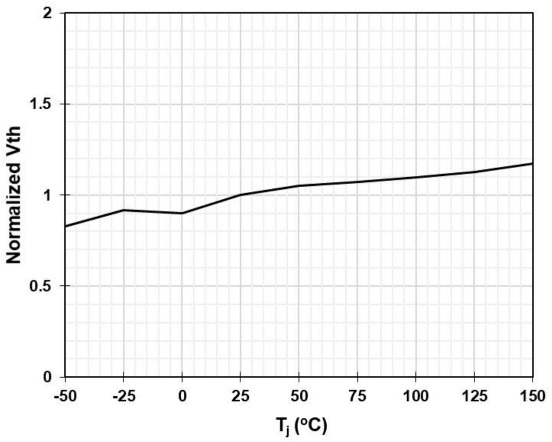
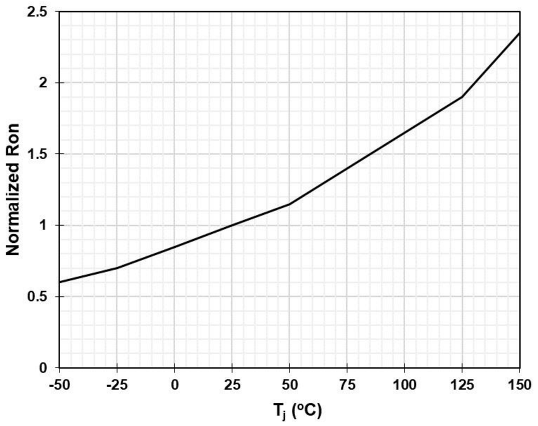
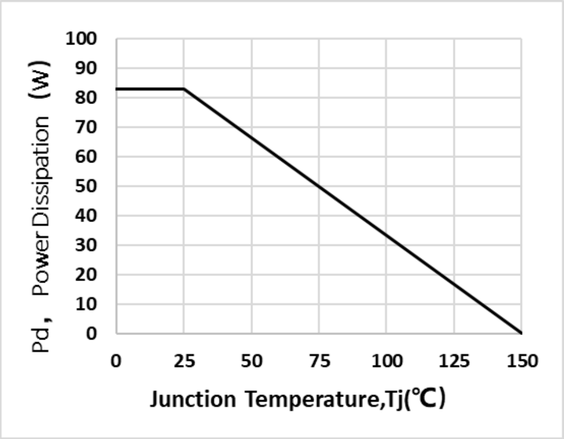
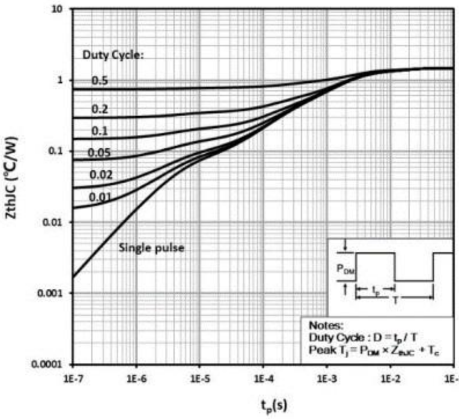
Figure 16 Gate threshold voltage	**Figure 17 Drain-source on-state resistance**
	
$V_{GS(TH)} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 11.4 mA	$R_{DS(on)} = f(T_j)$; I_D = 3.9 A; V_{GS} = 6 V

Figure 18 Power dissipation



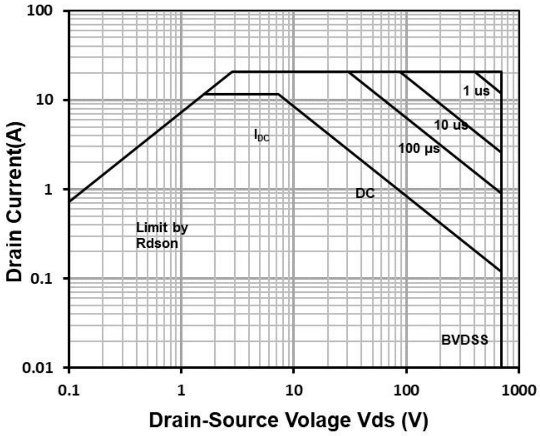
Ptot = f(Tc)

Figure 19 Max.transient thermal impedance



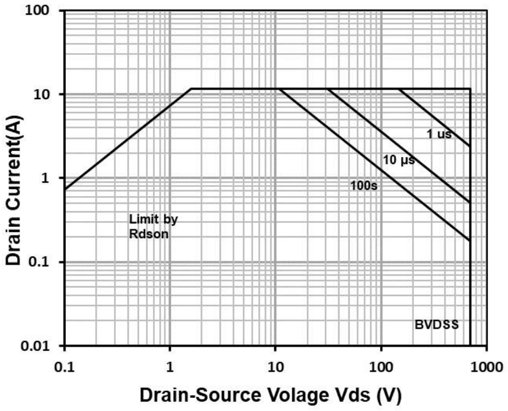
Zthjc = f(tp,D)

Figure 20 Safe Operation Area

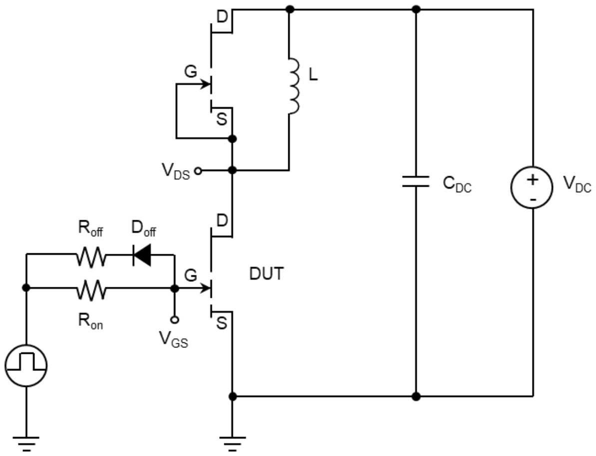
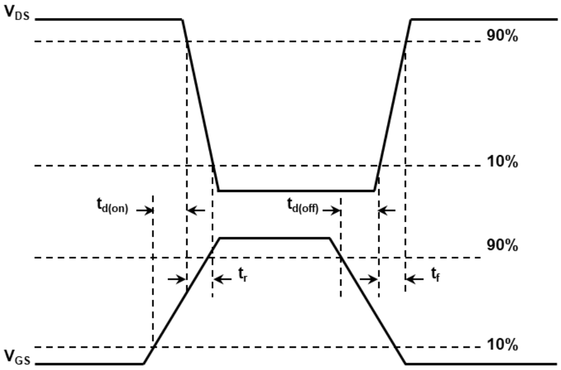


Id = f(Vds); Tc = 25℃

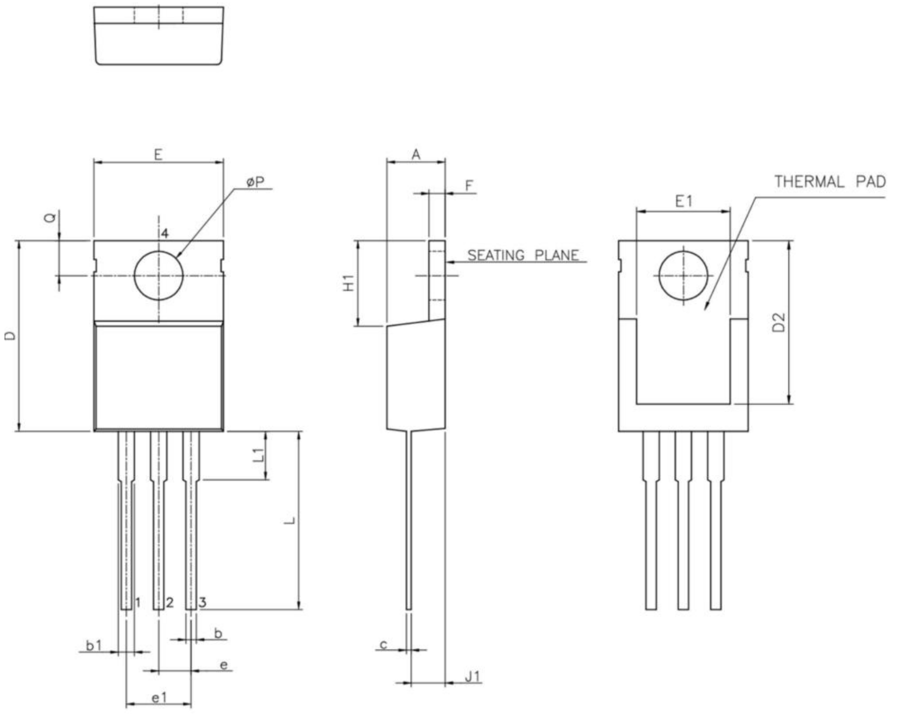
Figure 21 Safe Operation Area



Id = f(Vds); Tc = 125℃

Figure 22 Switching time test circuit	**Figure 23 Typ. switching time waveforms**
	
V_{DS} = 400 V, I_D = 8 A, L = 318 µH, V_{GS} = 6 V, R_{on} = 10 Ω, R_{off} = 2 Ω	

4 Package Information



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	3.56	4.82
b1	1.15	1.77
b	0.38	1.01
c	0.35	0.61
D	14.23	16.51
E	9.66	10.66
D2	11.75	11.90
E1	6.86	8.90
e	2.29	2.79
e1	4.83	5.33
F	0.51	1.39
H1	5.85	6.85
J1	2.04	2.92
L	12.70	14.73
øP	3.54	4.08
Q	2.54	3.42
L1	3.65	6.35

NOTES:
1. JEDEC OUTLINE : N/A.

5 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2026-04-27	Initial release

6 Further Information

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Data Source– Data here are based on recent tests but all parameters may not be up to date. Actual final test data from packaging production are available for selected customers upon request.