

GPI65005DF56

N-channel 650V 5A GaNPower HEMT in DFN 5X6 Package

Datasheet version 3.1

Features

BV_{DSS}	$R_{DS(on)}$	I_{DS}	Q_G
700 V	235 mΩ	5A	1.6 nC

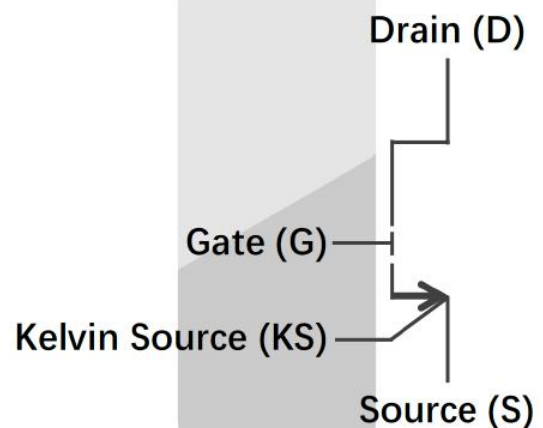
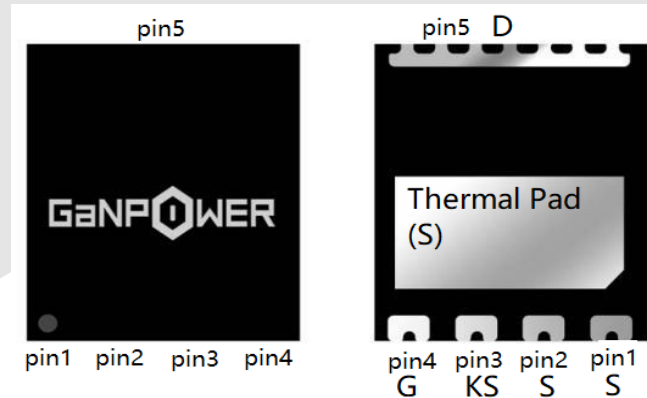
- Ultra-low $R_{DS(on)}$
- High dv/dt capability
- Extremely low input capacitance
- Zero Q_{rr}
- Outstanding switching performance
- Low Profile

Applications

- Switching Power Applications
- Server and Telecom Power Application
- EVOBC and DC-DC Converters
- UPS, Inverters, PV

Description

These devices are N-channel 650V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology. The resulting product has extremely low on state resistance, very low input capacitance and zero reverse recovery charge making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency.



Device Characteristics

Static Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$V_{GS(TH)}$	Gate threshold voltage	$V_{DS}=V_{GS}$, $I_D=3.5mA$ ($T_J=25\text{ }^{\circ}C$)	0.9	1.25	2.9	V
			$V_{DS}=V_{GS}$, $I_D=3.5mA$ ($T_J=150\text{ }^{\circ}C$)		1.15		V
2	BV_{DSS}	Drain-Source breakdown voltage	$V_{GS}=0V$, $I_D < 20\text{ }\mu A$ ($T_J=25\text{ }^{\circ}C$)		700		V
3	I_{DSS}	Zero gate voltage drain leakage current	$V_{GS}=0V$, $V_{DS}=650V$ $T_J = 25\text{ }^{\circ}C$		0.01	10	μA
			$V_{GS}=0V$, $V_{DS}=650V$ $T_J = 150\text{ }^{\circ}C$		3		μA
4	I_{GSS}	Gate-Source Leakage	$V_{GS}=6V$, $V_{DS}=0V$		13	500	μA
5	$R_{DS(on)}$	drain-source on resistance	$V_{GS}=6V$, $I_D=1A$ $T_J = 25\text{ }^{\circ}C$		235	320	m Ω
			$V_{GS}=6V$, $I_D=1A$ $T_J = 150\text{ }^{\circ}C$		580		m Ω
6	V_{SD}	Reverse conduction voltage	$I_{SD}=0.1A$, $V_{GS}=0V$	1.2	2.2	3	V
7	R_G	Gate resistance	f=25Mhz Open drain		1		Ω
Dynamic Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	C_{ISS}	Input capacitance	$V_{GS}=0V$		39		pf
2	C_{OSS}	Output capacitance	$V_{DS}=500V$		11.8		pf
3	C_{RSS}	Reverse transfer capacitance	f = 100 kHz		0.24		pf
4	$C_{O(ER)}$	Effective output capacitance, energy related	$V_{DS}=0-500V$		15		pf
5	Q_G	Gate charge	$V_{DS}=500V$		1.6		nC
6	Q_{GS}	Gate to source charge	$I_D=2.5A$		0.30		nC
7	Q_{GD}	Gate to drain charge	$V_{GS}=6V$		0.38		nC
8	Q_{OSS}	Output Charge	$V_{DS}=0-500V$		10		nC
9	Q_{RR}	Reverse recovery charge			0		nC

Switching Performance				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$t_{D(ON)}$	Turn-on delay time	$V_{DS} = 500\text{ V}$ $I_D = 1.25\text{ A}$ $R_G = 22/2\ \Omega$ $V_{GS} = -3/6\text{ V}$		5		ns
2	t_R	Rise time			10		ns
3	$t_{D(OFF)}$	Turn-off delay time			16		ns
4	t_F	Fall time			11		ns

Absolute Max. Ratings

	Symbols	Parameters	Value	Unit
1	V_{DS-max}	Breakdown voltage transient @ $T_{case}=25^\circ\text{C}$	800	V
2	V_{DS-max}	Breakdown voltage transient @ $T_{case}=125^\circ\text{C}$	650	V
3	V_{GS-max}	Gate to source max. voltage @ $T_{case}=25^\circ\text{C}$	-12 to +7.5	V
4	I_{DS-max}	Drain to source DC current @ $T_{case}=25^\circ\text{C}$	5	A
5	I_{DS-max}	Drain to source pulse current @ $T_{case}=25^\circ\text{C}$, pulse width 10 μs , $V_{GS} = 6\text{ V}$	11	A
6	I_{DS-max}	Drain to source pulse current @ $T_{case}=100^\circ\text{C}$	5	A
7	$dv/dt-max$	Drain to source voltage slew rate	150	V/ns
8	T_J-max	Max junction temperature	150	$^\circ\text{C}$
9	$T_S-storage$	Storage temperature	-55 to 150	$^\circ\text{C}$

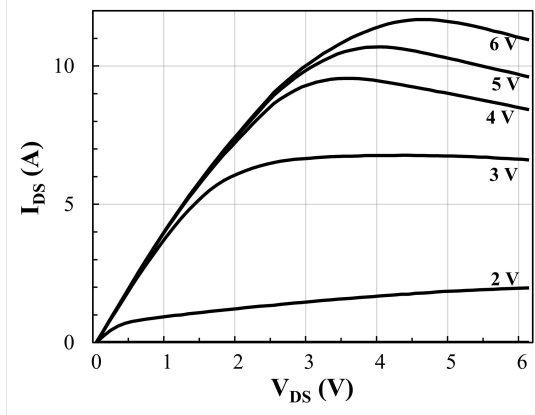
Thermal and Soldering Characteristics (Typical)

	Symbols	Parameters	Value	Unit
1	R_{thJC}	Thermal resistance (junction to case)	1.4	$^\circ\text{C}/\text{W}$
2	R_{thJA}	Thermal resistance (junction to ambient)	62	$^\circ\text{C}/\text{W}$
3	T_{solder}	Reflow soldering temperature	260	$^\circ\text{C}$

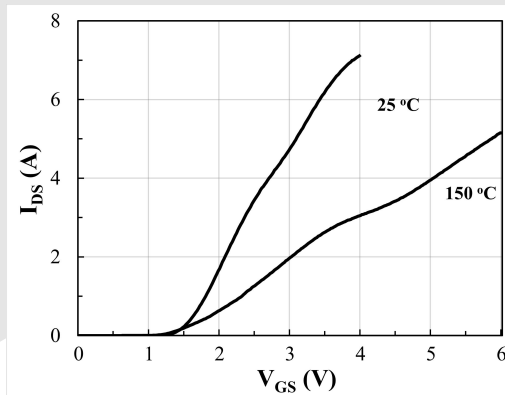
Ordering

Order Code	Package Type	Packaging Method	Qty
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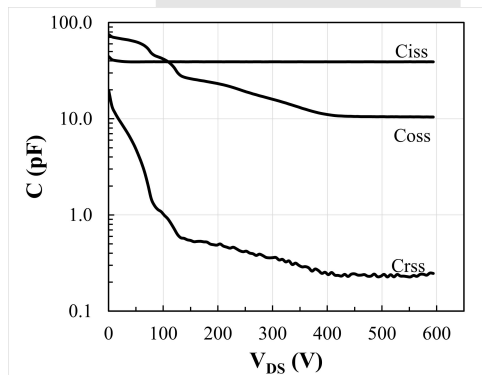
Electrical Performance



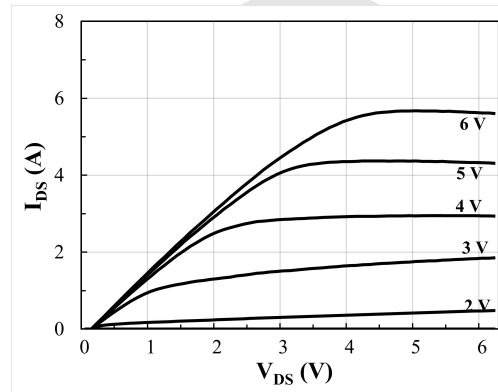
I_{DS} vs. V_{DS} @ $T_J = 25^\circ\text{C}$



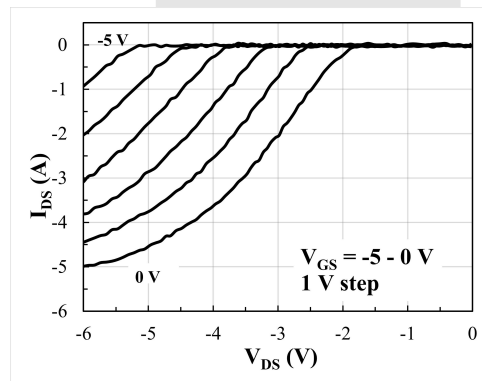
I_{DS} vs. V_{GS} @ $T_J = 25^\circ\text{C}$ and 150°C



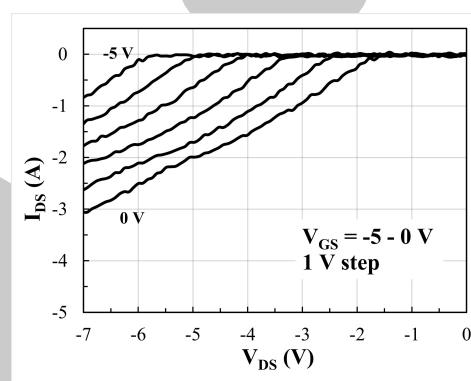
Capacitance vs. V_{DS} Curve @ $T_J = 25^\circ\text{C}$



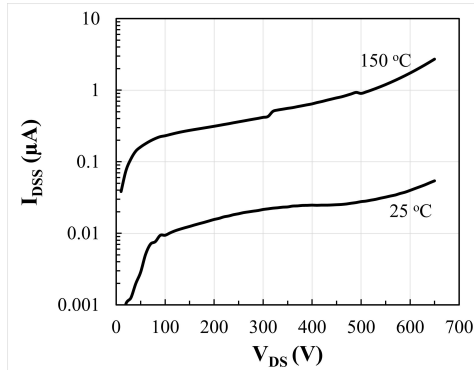
I_{DS} vs. V_{DS} @ $T_J = 150^\circ\text{C}$



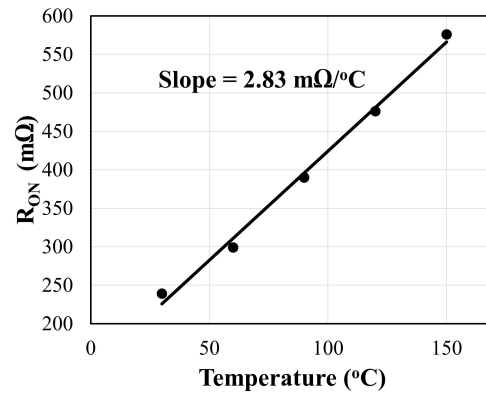
I_{SD} vs. V_{SD} reverse conduction curve @ $T_J = 25^\circ\text{C}$



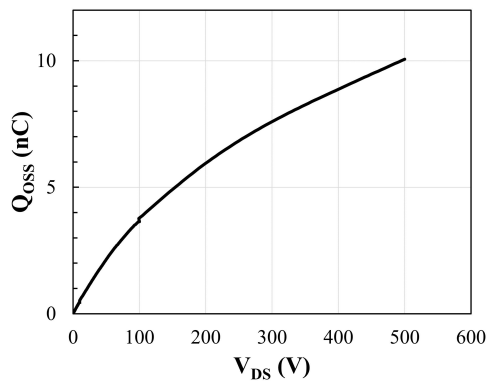
I_{SD} vs. V_{SD} reverse conduction curve @ $T_J = 150^\circ\text{C}$



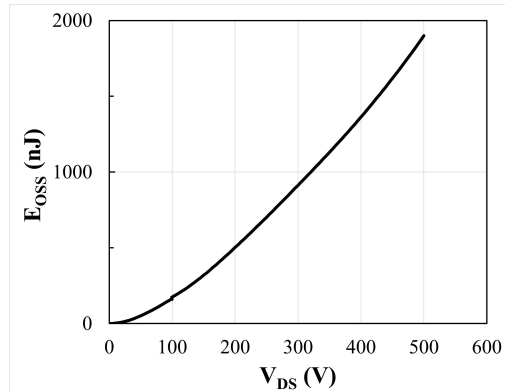
Typical off-state drain leakage current I_{DSS} vs. V_{DS} @ $T_J = 25^\circ C$ and $150^\circ C$



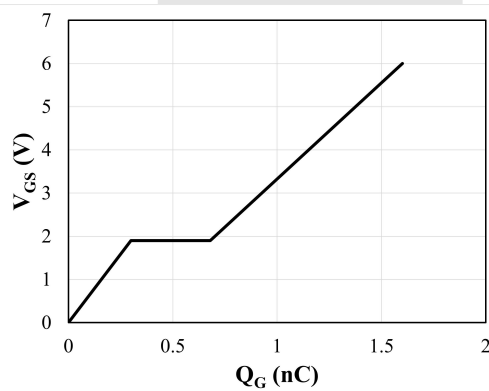
On-state resistance vs. T_J @ $I_D = 2.5\text{ A}$, $V_{GS} = 6\text{ V}$



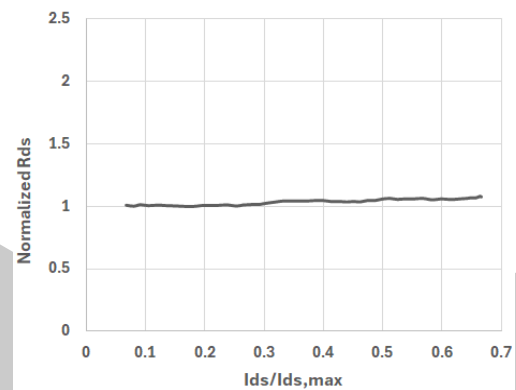
Output charge Q_{OSS} vs. V_{DS}



Stored Energy Characteristic E_{OSS} vs. V_{DS}

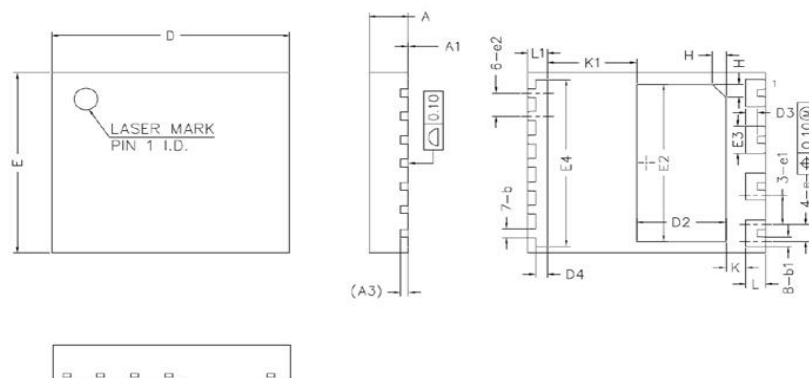


Gate charge V_{GS} vs. Q_G



Normalized $R_{DS(on)}$ vs. I_{DS} @ $T_J = 25^\circ C$

Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
A3	0.203REF		
b	0.20	0.25	0.30
b1	0.225	0.275	0.325
D	5.90	6.00	6.10
E	4.90	5.00	5.10
D2	2.15	2.25	2.35
E2	4.27	4.37	4.47
D3	0.20	0.30	0.40
E3	0.65	0.75	0.85
D4	0.20	0.30	0.40
E4	4.525	4.625	4.725
e	0.375	0.475	0.575
e1	0.725	0.825	0.925
e2	0.55	0.65	0.75
H	0.35REF		
K	0.35	0.50	0.65
K1	2.10	2.25	2.40
L	0.40	0.50	0.60
L1	0.40	0.50	0.60



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Further Information

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Data Source— Data here are based on recent tests but all parameters may not be up to date. Actual final test data from packaging production are available for selected customers upon request.