

# Wafer datasheet

Star120

(900V/120A)

(650V/120A)

## Features

**Choice of original 6V gate driving or  
0-12 or 0-15V regulated gate driving**

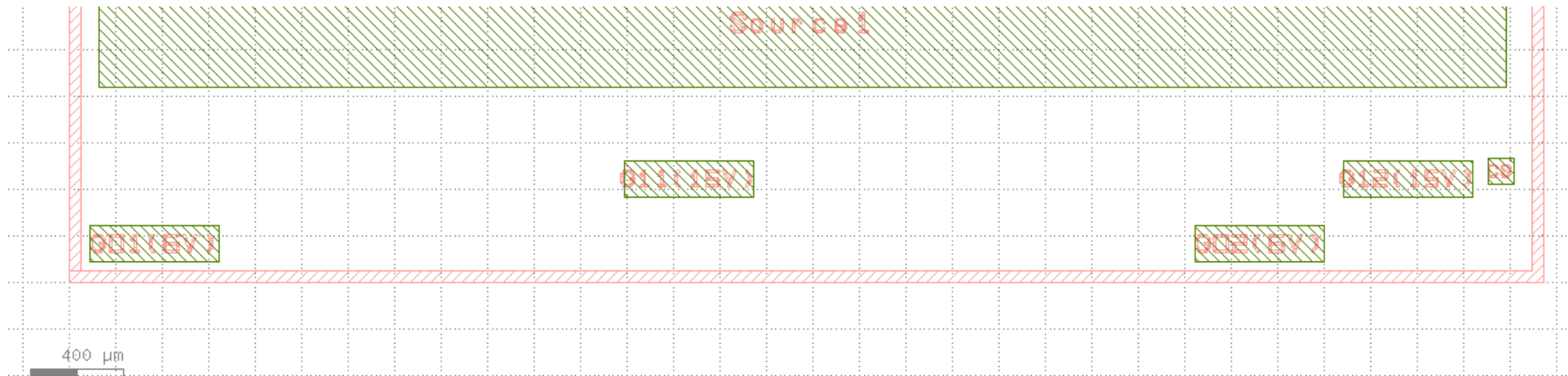
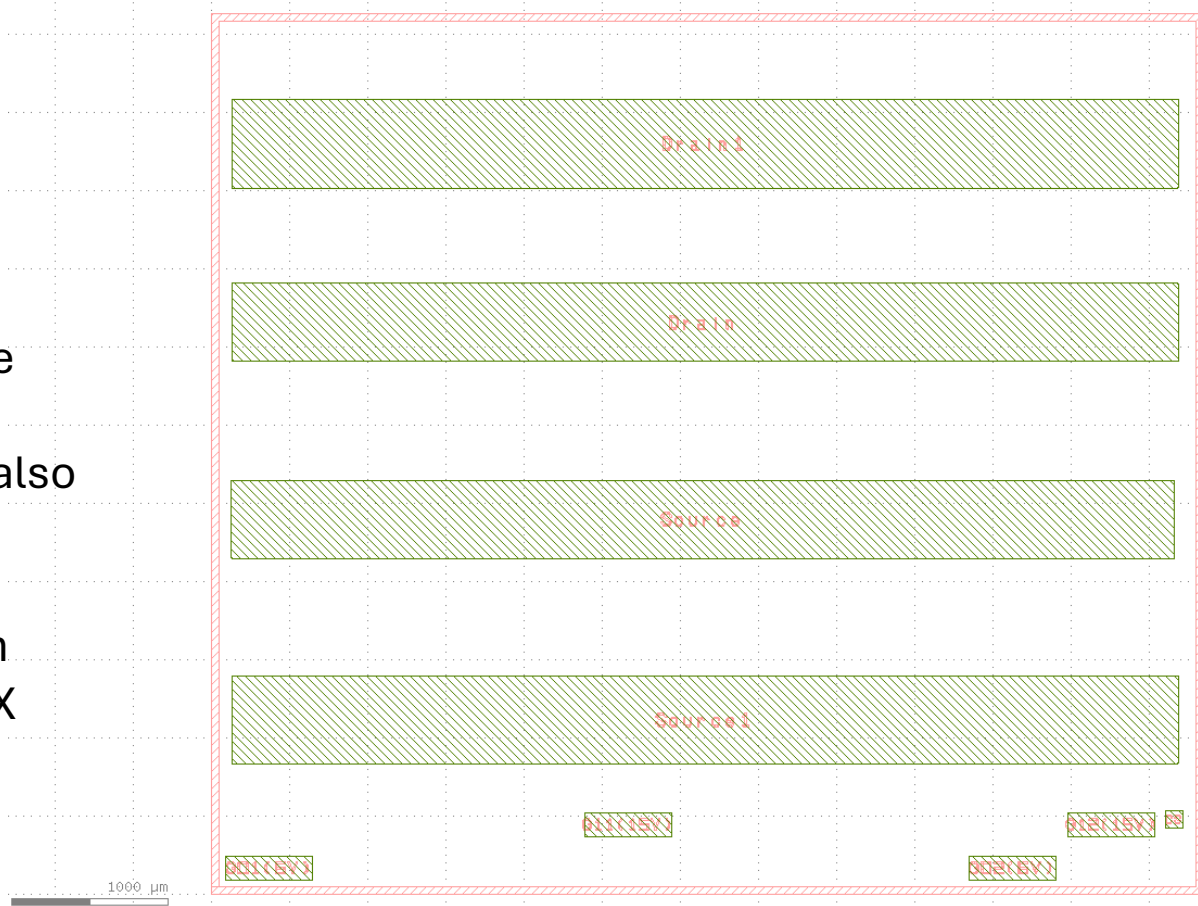
**Regulated gate driving enables anti-ringing  
Protection / ESD protection**

**Lossless source side current sensing**

Device-name	x-size	y-size
Star120	6345.90	5634.28

Note that G11(15V) and G12(15V) are internally connected.  
 Similarly, G01(6V) and G02(6V) are also internally connected.

For best gate control uniformity, both G1X (for 12/15V driving) or both G0X (for 6V driving) shall be used if wire bonding configuration allows.



**Main switch FET channel width: 1,426,822 um**

<b>PAD</b>	<b>Dx</b>	<b>Dy</b>	<b>Center_x</b>	<b>Center_y</b>
<b>G01(6V)</b>	<b>555.00</b>	<b>155.00</b>	<b>368.30</b>	<b>168.30</b>
<b>G11(15V)</b>	<b>585.00</b>	<b>185.00</b>	<b>2664.55</b>	<b>446.30</b>
<b>Source</b>	<b>6032.72</b>	<b>500.00</b>	<b>3144.16</b>	<b>2397.14</b>
<b>Source1</b>	<b>6053.72</b>	<b>560.00</b>	<b>3156.66</b>	<b>1116.70</b>
<b>Drain</b>	<b>6053.72</b>	<b>500.00</b>	<b>3156.66</b>	<b>3657.14</b>
<b>Drain1</b>	<b>6053.72</b>	<b>567.00</b>	<b>3156.66</b>	<b>4799.98</b>
<b>CS</b>	<b>111.00</b>	<b>111.00</b>	<b>6158.02</b>	<b>479.30</b>
<b>G02(6V)</b>	<b>555.00</b>	<b>155.00</b>	<b>5121.95</b>	<b>168.30</b>
<b>G12(15V)</b>	<b>585.00</b>	<b>185.00</b>	<b>5759.20</b>	<b>446.30</b>

# Basic specifications

Back metal	None
Front metal	AlCu 4um
Wafer diameter	6 inch
Wafer thickness before dicing	1000 um
Recommended die thickness after dicing	250-300um
Street width	80 um
Recommended storage	N2 environment

# Wire bonding suggestion

Larger pads use 10mil or 12mil Al .

Smaller pads use Cu, PdCu , or Au (1.5 mil – 2 mil)

Backside must be glued to backplate using conductive glue

Backplate must be connected to the source of the GaNFET using wire bonding

# Characteristics

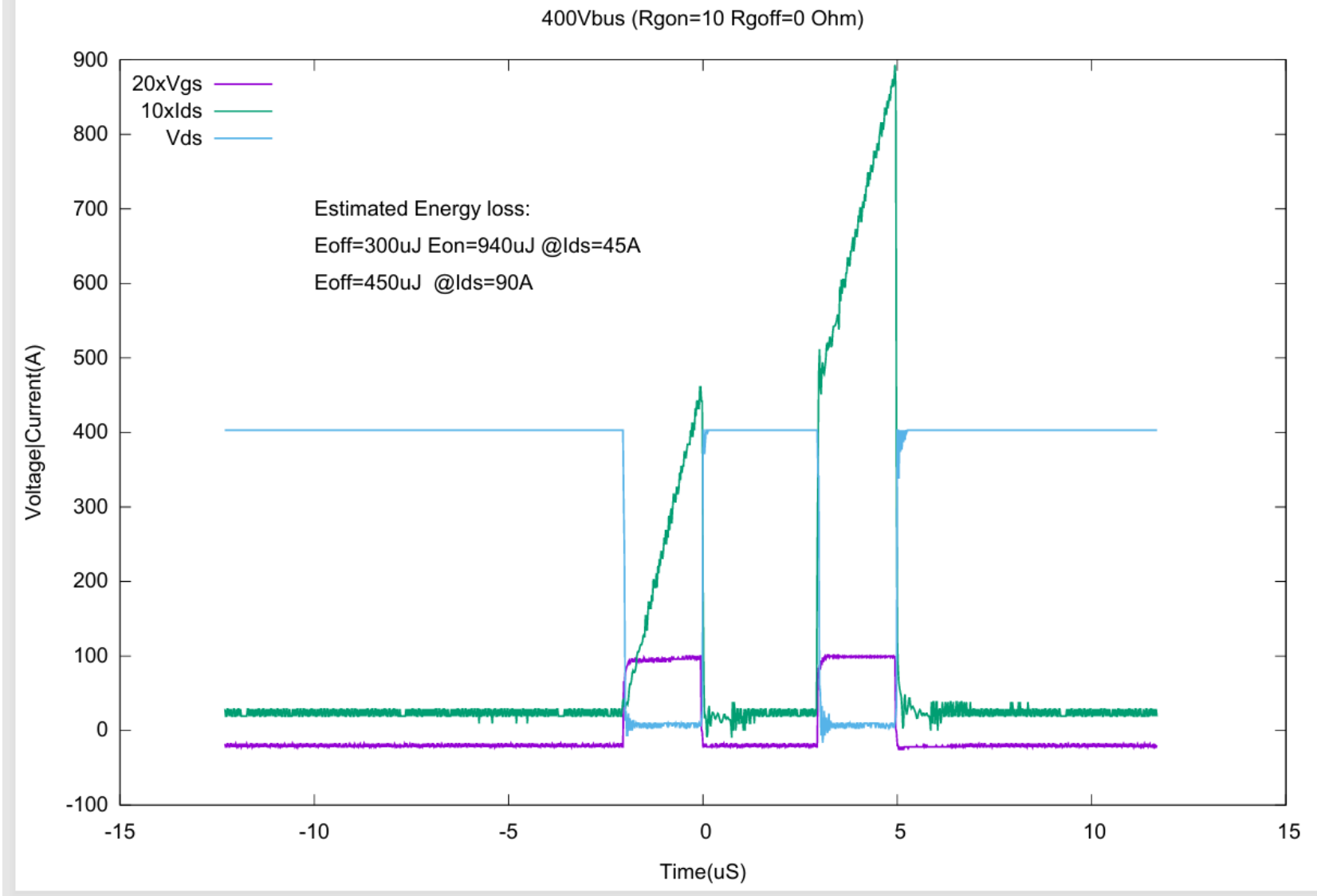
		Condition	min	typical	max	
I <sub>ds</sub> -max	Max current at 125C	V <sub>gs</sub> =6/15 125C		120		A
I <sub>ds</sub> -max	Max current at 25C	V <sub>gs</sub> =6/15 25C		240		A
V <sub>ds</sub> -max	D-S breakdown voltage	V <sub>gs</sub> =0 25C < 100uA		900		V
V <sub>g0s</sub>	Original gate voltage		-3		7	V
V <sub>g1s</sub>	Regulated		-20		20	
V <sub>gth</sub> (G0)	Gate threshold voltage	V <sub>gs</sub> =V <sub>ds</sub> I <sub>ds</sub> =35mA		1.3		V
V <sub>g1th_lin</sub> (G1)	Regulated threshold	V <sub>ds</sub> =0.01V, I <sub>ds</sub> =100 mA	2.64	3.95	5.26	V
V <sub>g1th_sat</sub> (G1)	Regulated threshold	V <sub>ds</sub> =0.01V, I <sub>ds</sub> =100 mA		2.09	3.75	V
R <sub>dson</sub>	On resistance	V <sub>g0s</sub> =6/V <sub>g1s</sub> =15 I <sub>ds</sub> =1A 25C	8.4	12	16	mOhm
R <sub>dson</sub> (150C)	On resistance	V <sub>g0s</sub> =6/V <sub>g1s</sub> =15 I <sub>ds</sub> =1A 150C	18	26	34	mOhm
V <sub>cs</sub>	Current sensing	I <sub>ds</sub> =+/-120A	-2.5		2.5	V
Q <sub>g</sub>	Gate charge	V <sub>bus</sub> =500V Turn-off from I <sub>ds</sub> =60A V <sub>g0s</sub> from 6 to 0 25C		29		nC

		Condition	min	typical	max	
Gm-Max	Max transconductance		360	650		mS
IDSS	Drain leakage	Vg1s=0 / Vg0s=0 Vds=800 25C		3.8	10	uA
IDSS(150C)	Drain leakage	Vg1s=0 / Vg0s=0 Vds=850 150C		19	75	μA
IDSS(150C)	Drain leakage	Vg1s=0 / Vg0s=0 Vds=900 150C		33	85	μA
IGSSF	Forward gate leakage	Vg1s=6 Vds=0 25C		670	5500	μA
-IGSSR	Reverse gate leakage	Vg1s=-6 Vds=0 25C		0.2	0.8	μA
-IGSSR(150C)	Reverse gate leakage	Vg1s=-6 Vds=0 150C		131	930	uA
Max_Isoff	Source leakage	Vg=Vs=Vb=GND, Vd=800V		0.6	7	μA
Isub	Bulk/substrate leakage	Vs=Vg=Vd=800V, B=GND		4.3		μA



## Gate pulsing test at 200KHz (4 uS on /1 uS off)

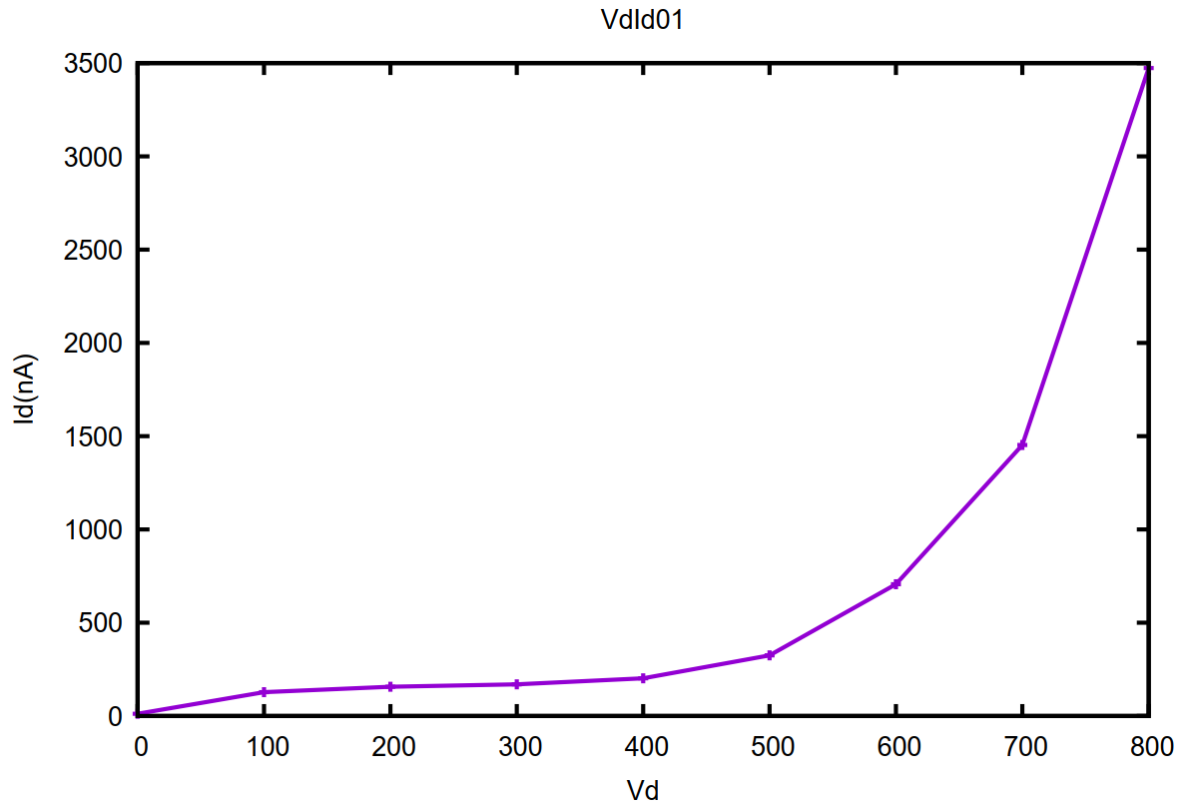
VG1(-)	VG1(+)	VG0(-)	VG0(+)	VBUS
-1.3	11.6	-0.7	7.4	0
-3.4	11.6	-3.1	7.4	0
-6.3	11.6	-6.3	7.4	0
-3.4	11.6	-3.0	7.4	100V (1.5A)
-3.4	11.6	-2.9	7.4	200V (2.1A)
-3.4	11.6	-2.8	7.4	400V (4.5A)



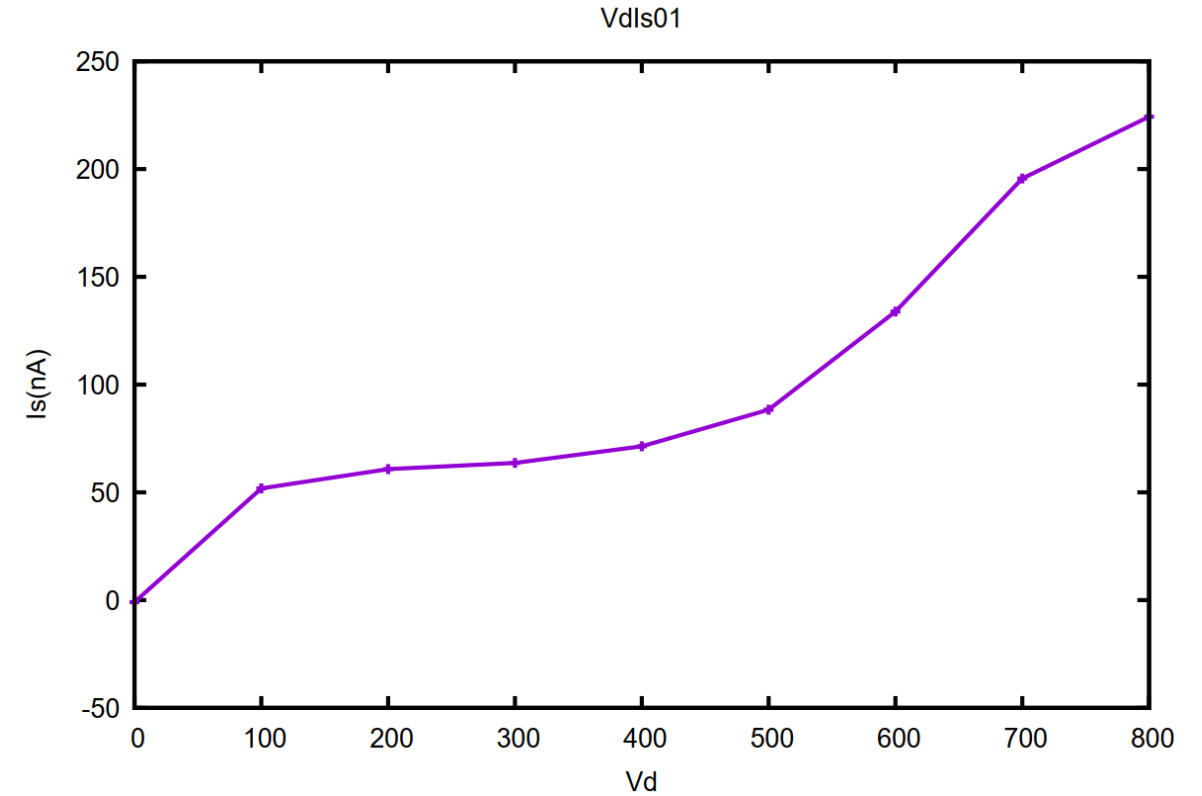
Dynamic test using TO247-4 package

For more realistic evaluation of power integral, ringing in  $I_{ds}(t)$  data have been eliminated by peak to peak averaging.

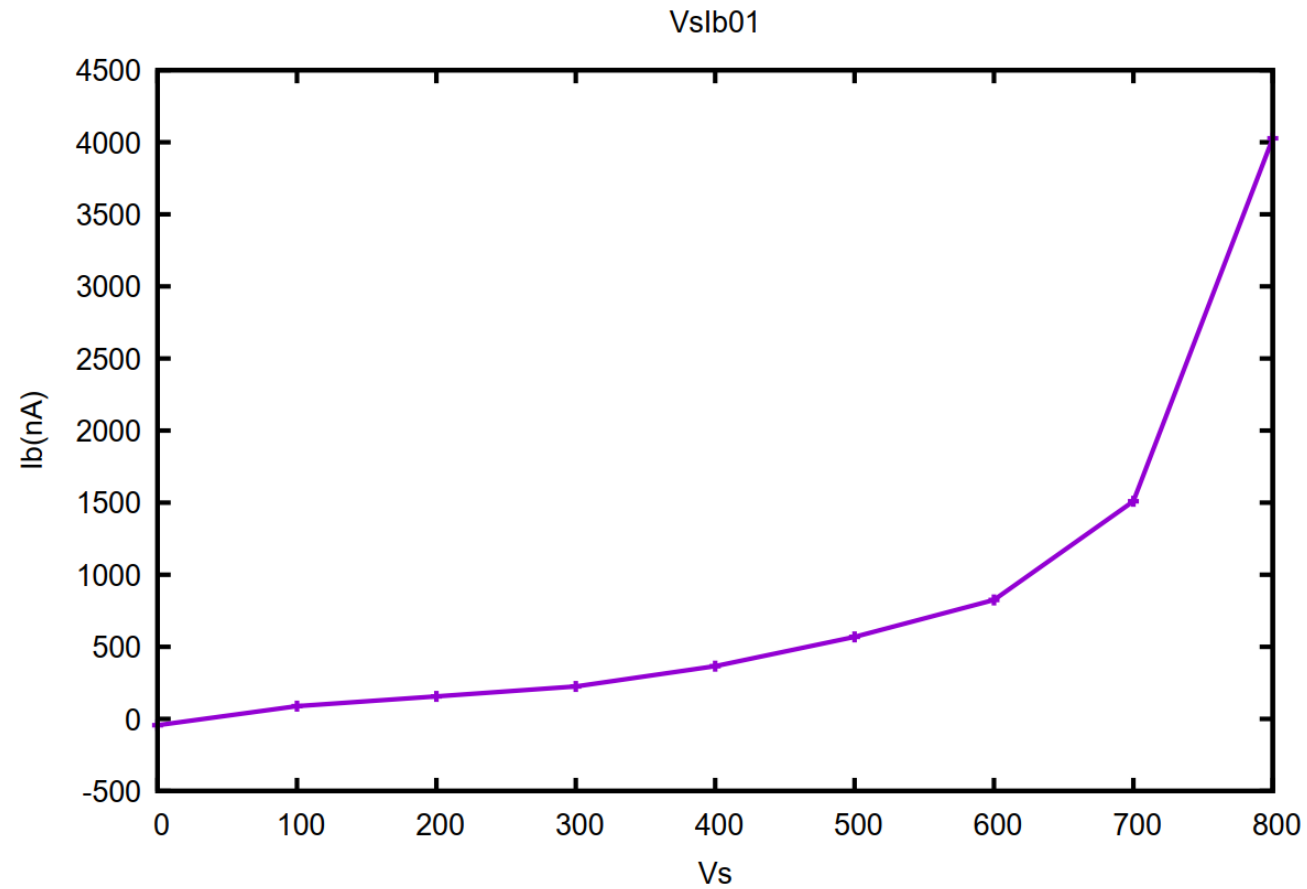
# @RT



**Drain leakage  $I_{dss}$  versus  $V_{ds}$   
@ $V_g=V_s=V_b=GND$**

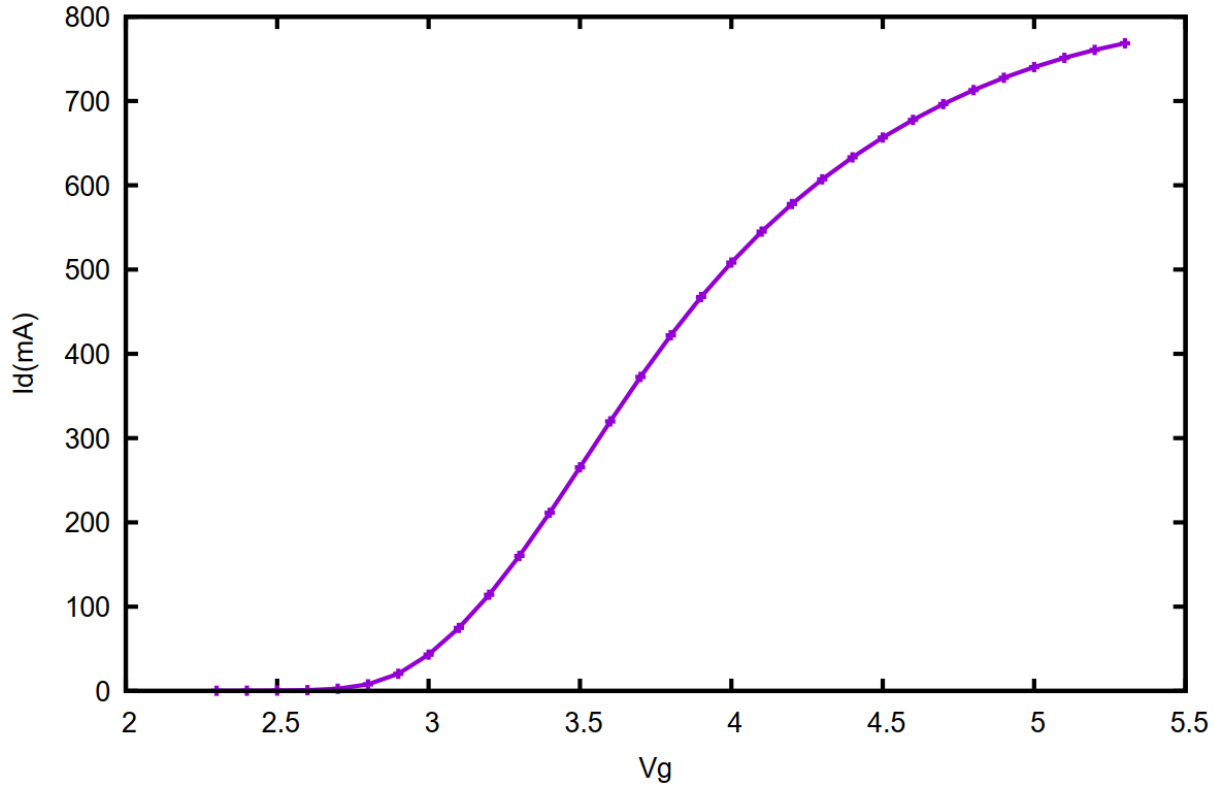


**Source leakage  $I_s$  versus  $V_{ds}$   
@ $V_g=V_s=V_b=GND$**



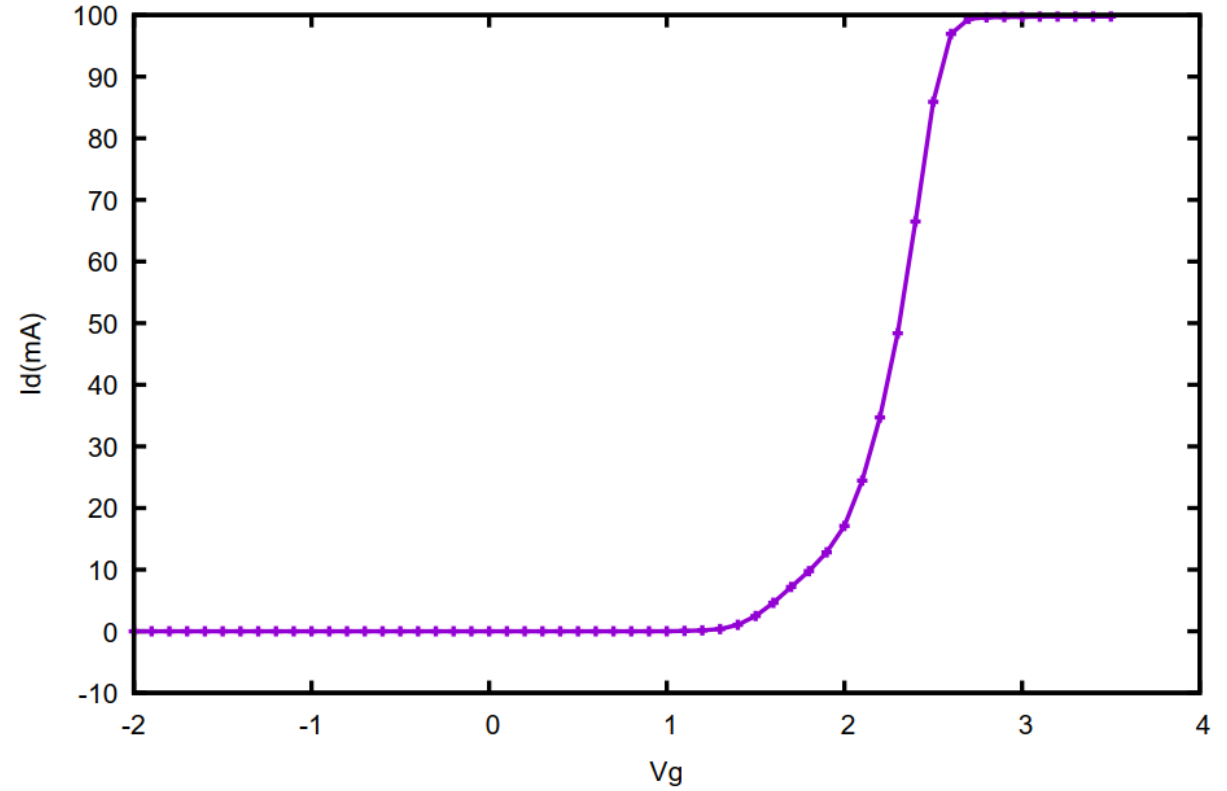
**Bulk (Substrate) leakage  $I_b$  versus  $V_s$   
@ $V_g=V_s=V_d$ , B=GND**

VgId03

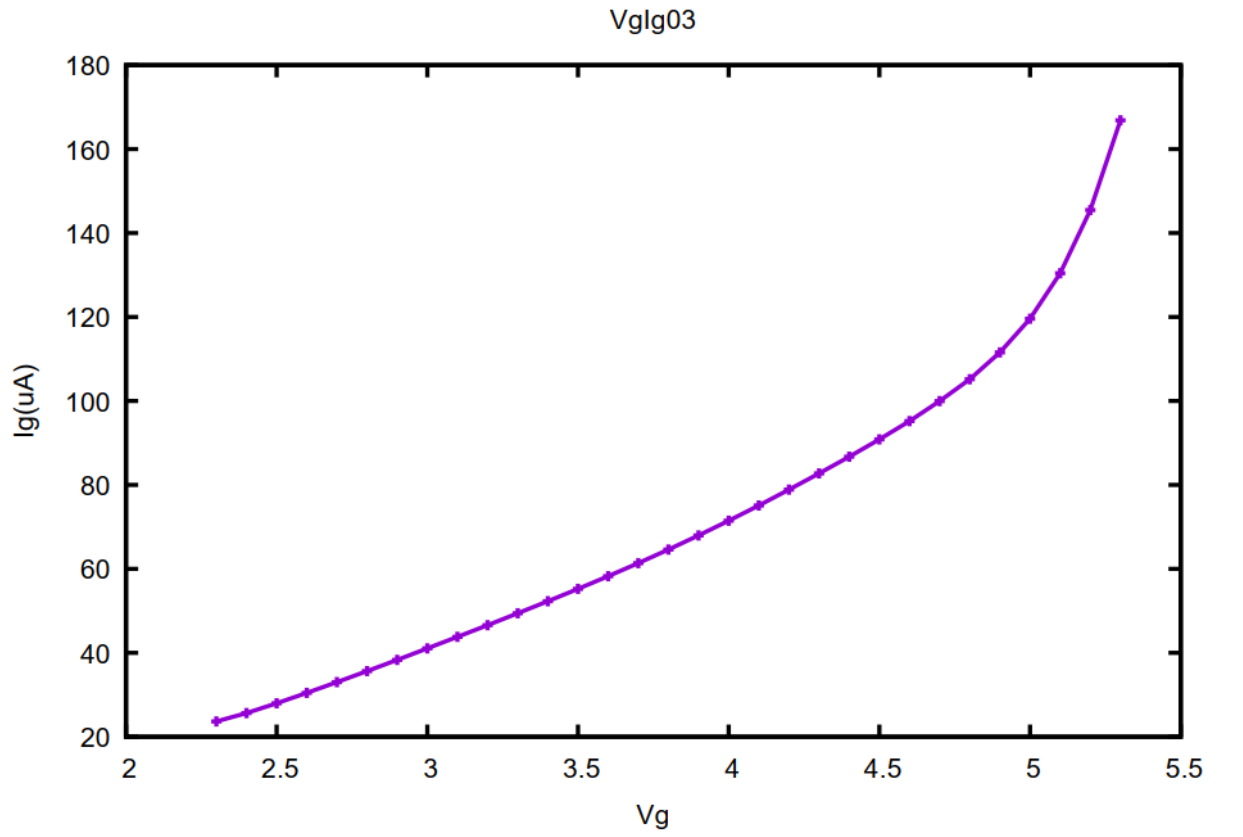
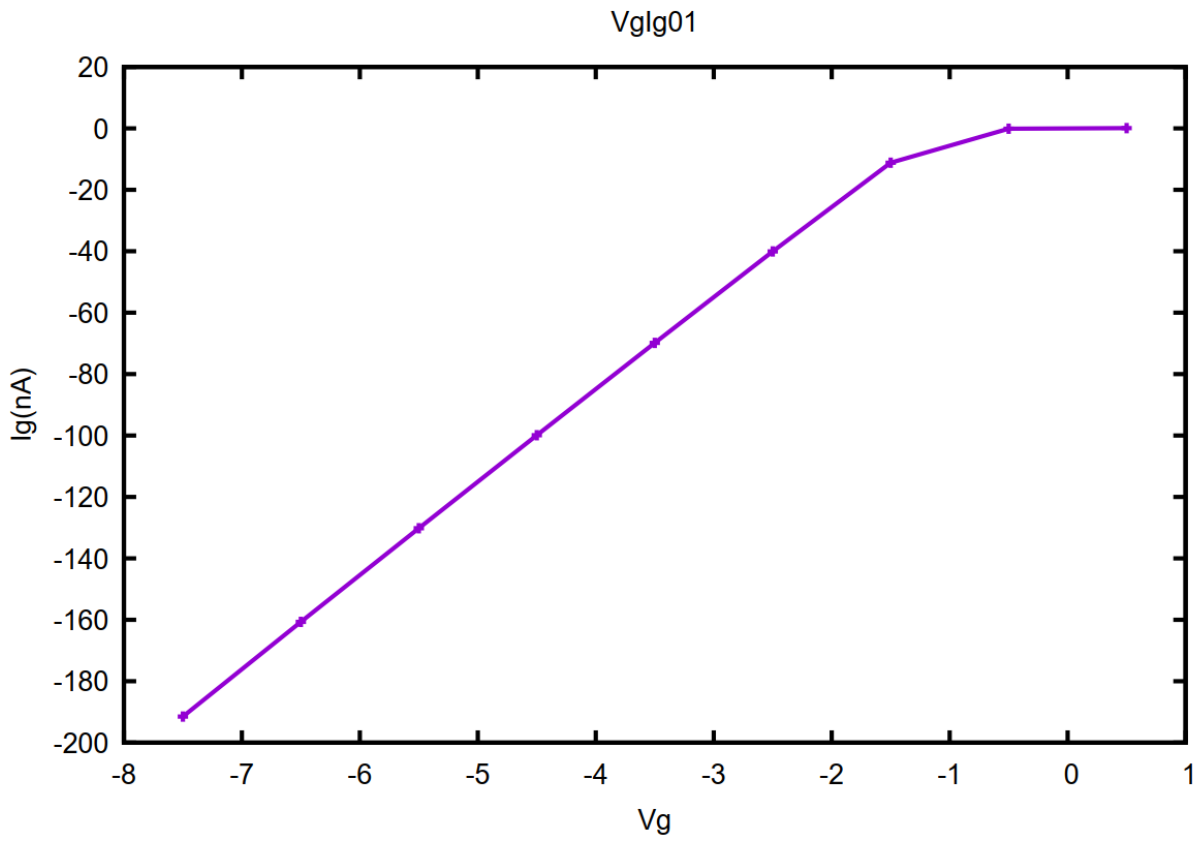


**Id-Vg transfer curve**  
**@Vds=0.01V, Vs=Vb=GND**

VgId04

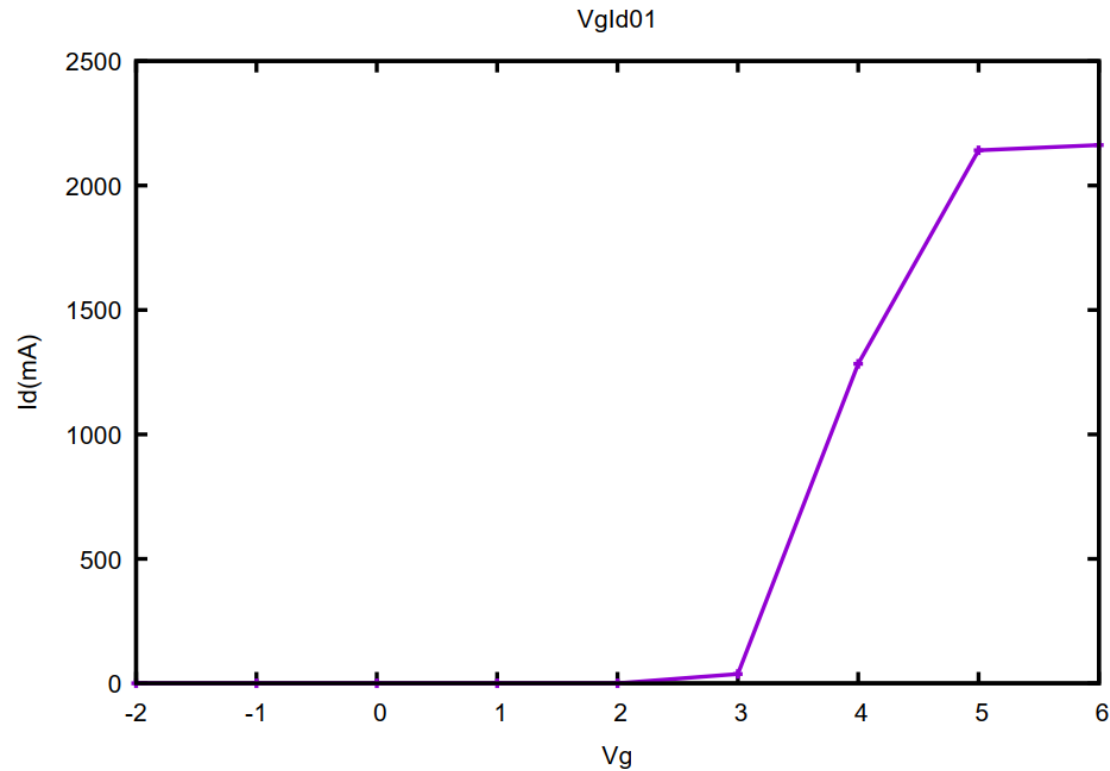


**Id vs Vg transfer curve**  
**@Vds=100V, Vs=Vb=GND**

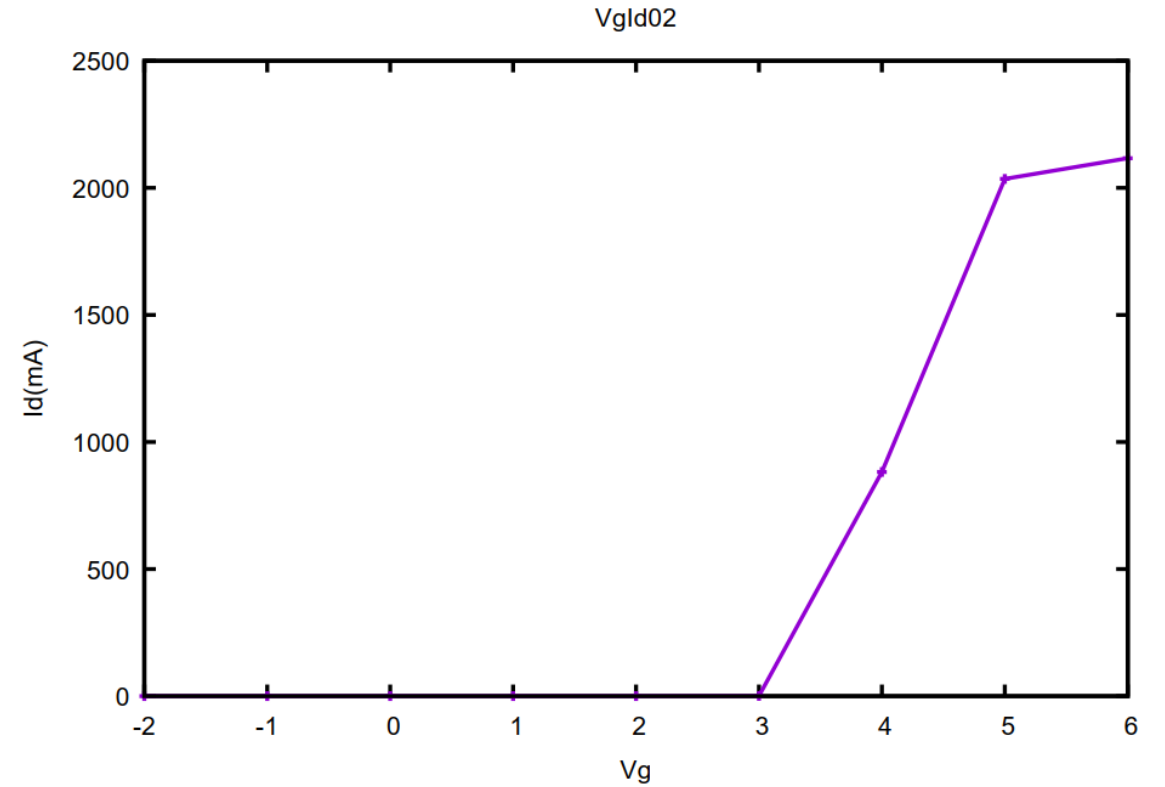


**Gate leakage**  
**@ $V_{ds}=0.1$ V,  $V_s=V_b=GND$**

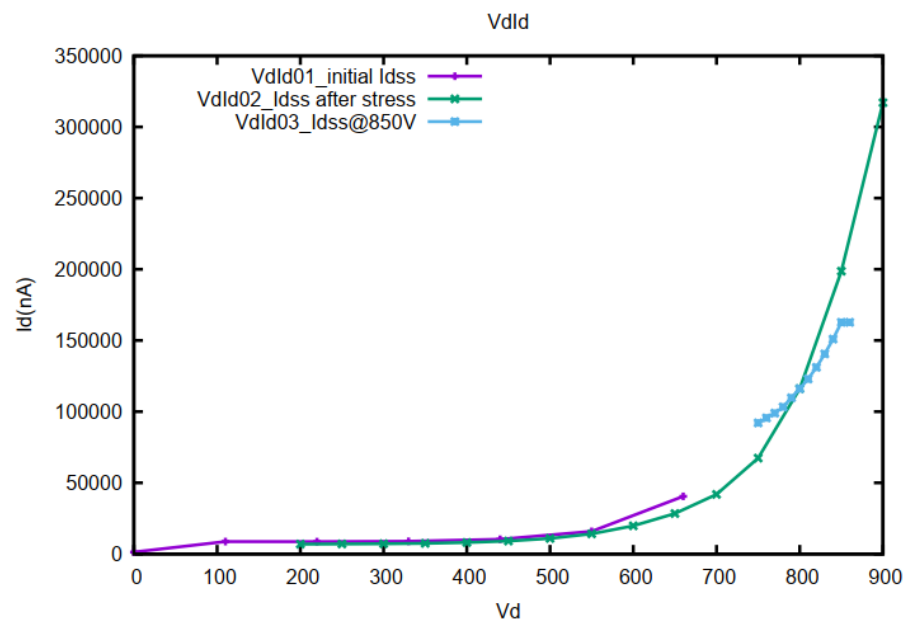
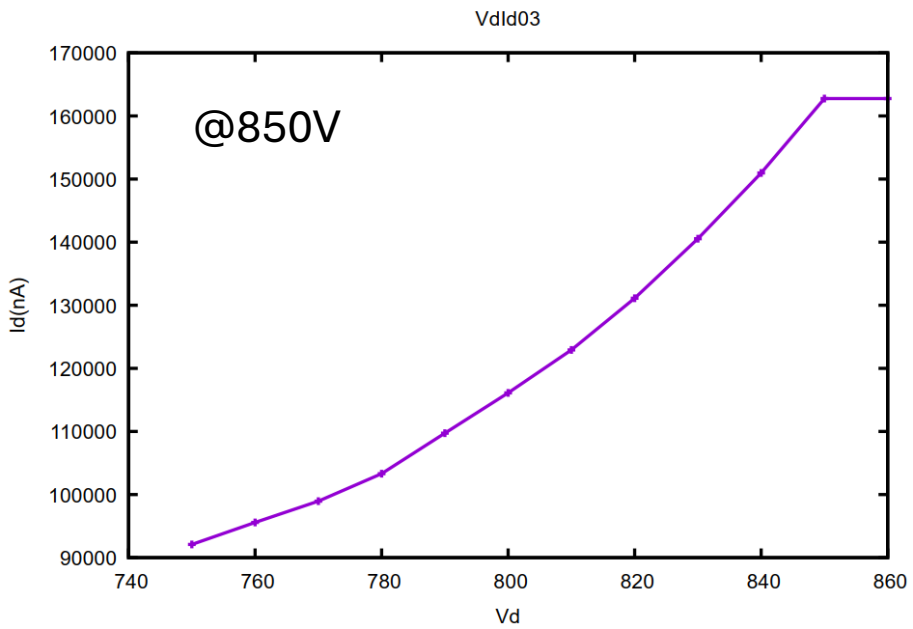
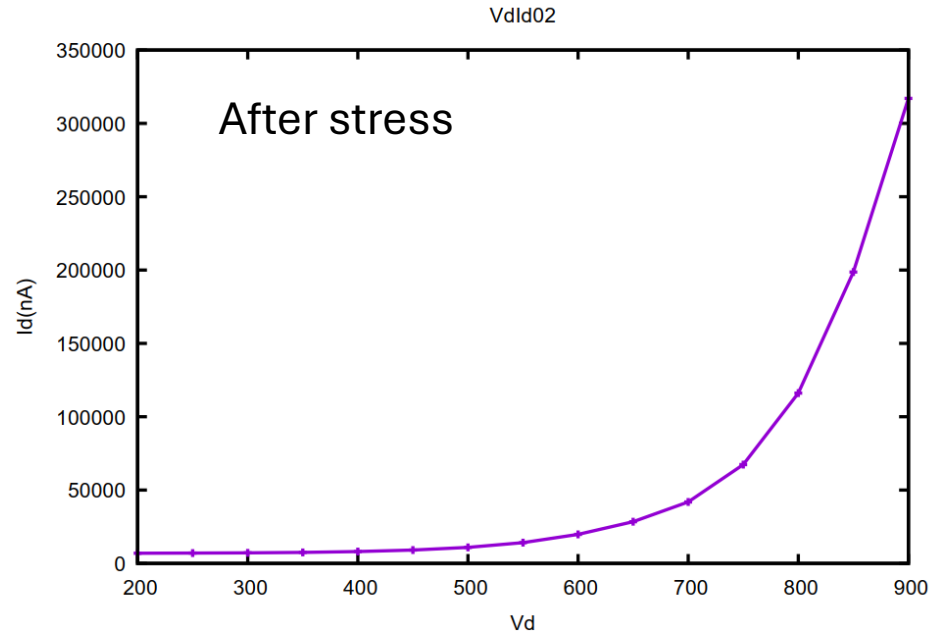
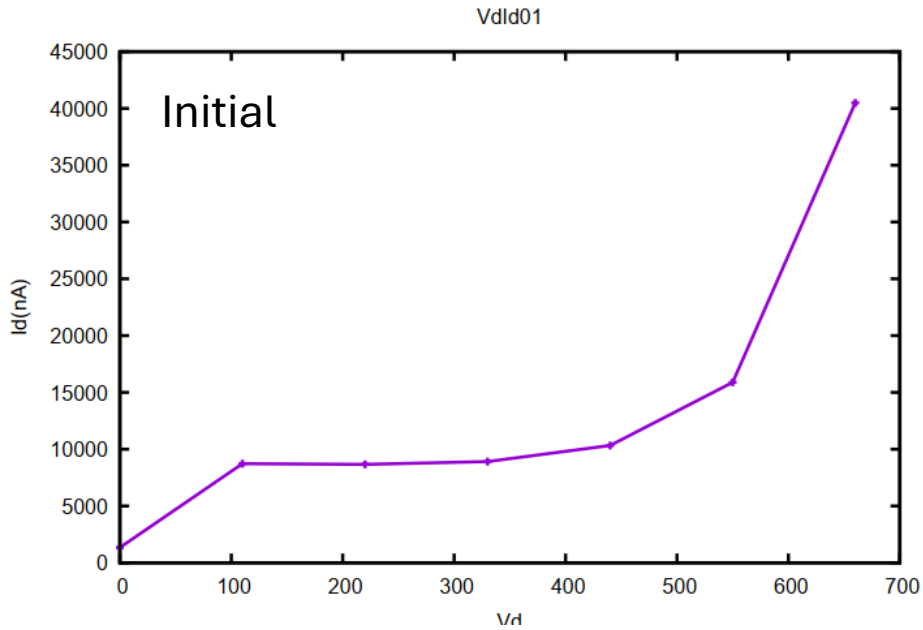
# @HT 150 °C



**Id-Vg transfer curve, initial @Vds=0.1V**

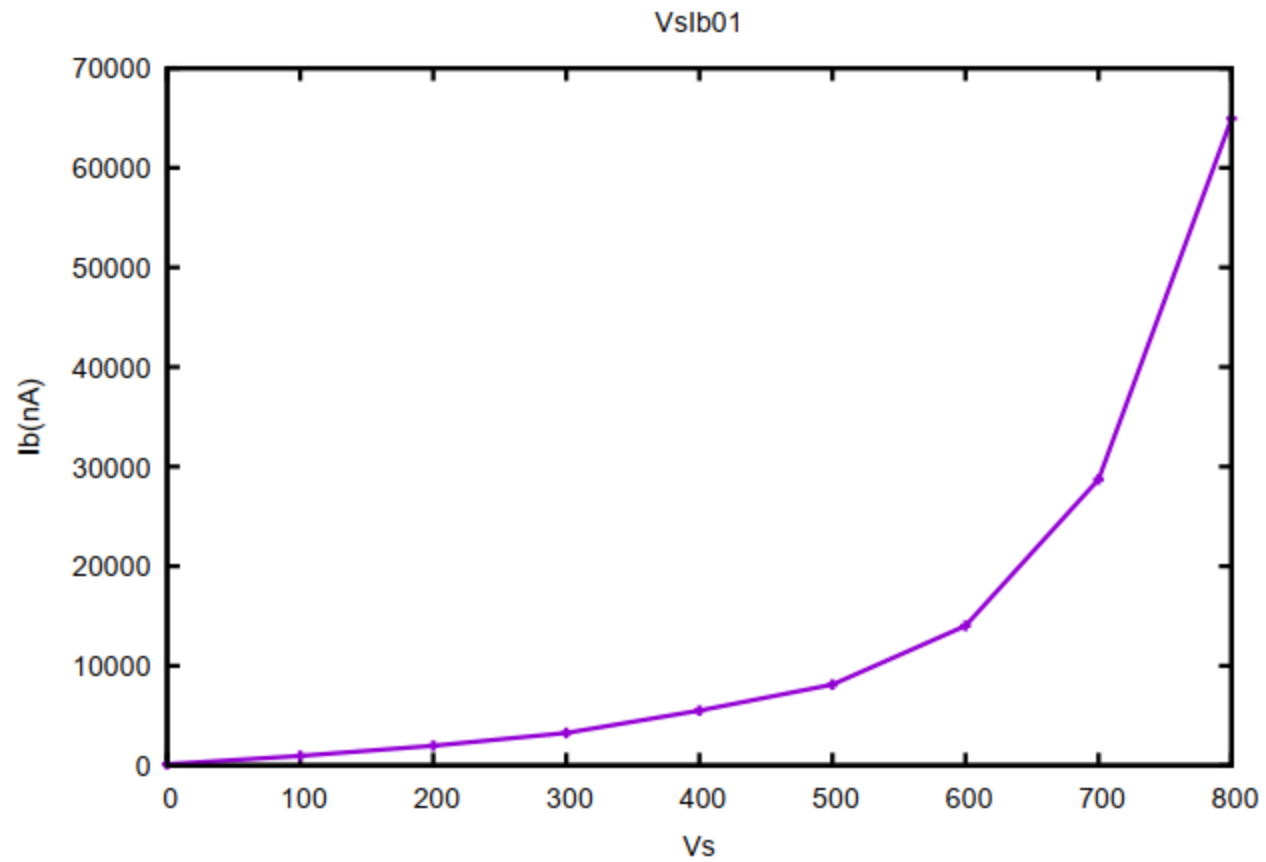


**Id-Vg transfer curve, after stress @Vds=0.1V**



**Drain leakage  $I_{dss}$  versus  $V_d$  @ $V_g=V_s=V_b=GND$**





**Bulk/substrate leakage  $I_b$  versus  $V_s$   
@ $V_g=V_s=V_d$ ,  $B=GND$**

# Application note on G1 (15V) driving

When using G1 for driving (either 0-12V or 0-15V):

Best to wire bond a bare die of low voltage diode (max rating 20V, max current 0.5A) between G0 and G1 such that the forward direction of the diode points from G0 to G1.

G1 comes with ESD protection and anti-ringing protection.

Recommended  $R_{goff}=0$   $R_{gon}=0$  to 5 Ohm.

# Application note on G0 (6V) driving

G0 is unprotected against ESD at this version and can be used as a standard EMODE p-GaN gate.

Recommended  $R_{goff}=0$   $R_{gon}=5-10$  Ohm