

GP120R90DF88

N-channel 1200V 20A GaN Power HEMT in DFN88 Package

Preliminary Datasheet version: 1.0

Features

V_{DSS}	R_{dson}	I_{ds}	V_{GS}	$V_{GS(TH)}$
1200V	90mΩ	20A	-1V to 15V	3.7 V

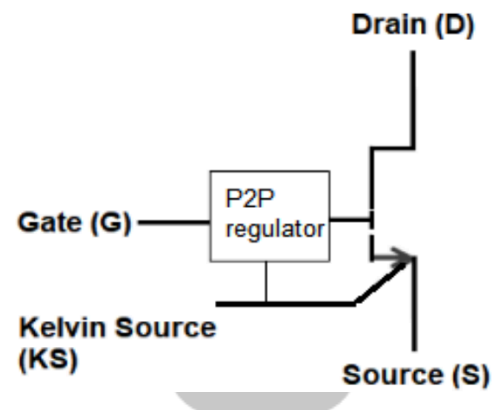
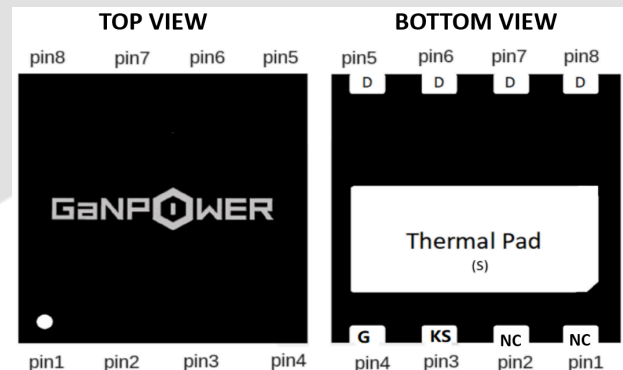
- Ultra-low R_{DSON}
- High dv/dt capability
- Extremely low input capacitance
- Zero Qrr
- Outstanding switching performance
- Low Profile
- **Upgraded P2P GaN with input regulator IC to match input lead and voltage of existing SiC MOSFET**

Applications

- Switching Power Applications
- Server and Telecom Power Application
- EV OBC and DC-DC Converters UPS, Inverters, PV

Description

These devices are N-channel 1200V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology, integrating an input regulator circuit to match input lead and voltage of existing SiC MOSFET in a pin-to-pin (P2P) fashion. The resulting product has extremely low on-state resistance, very low input capacitance and zero reverse recovery charge, making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency.





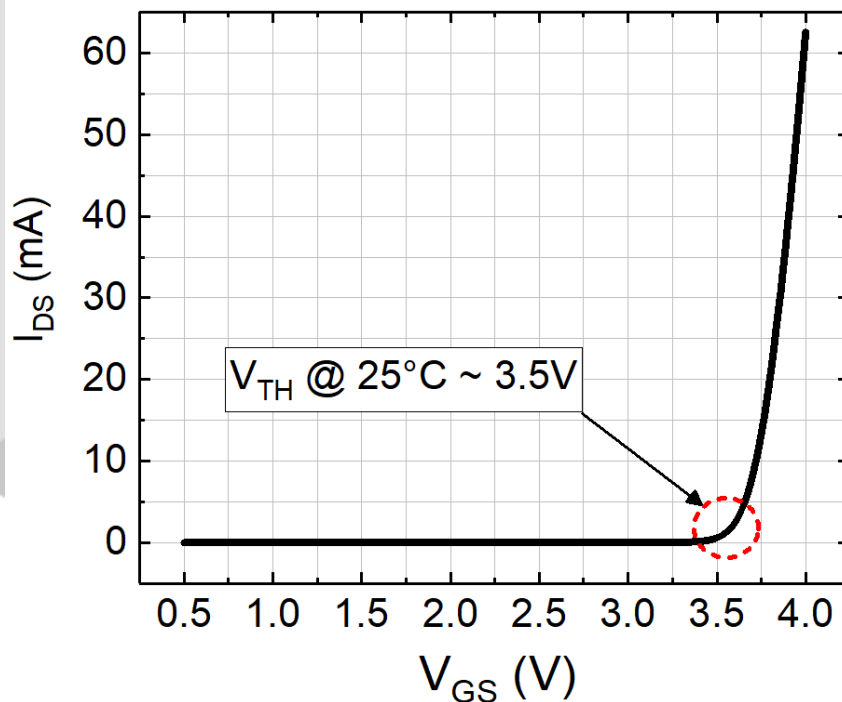
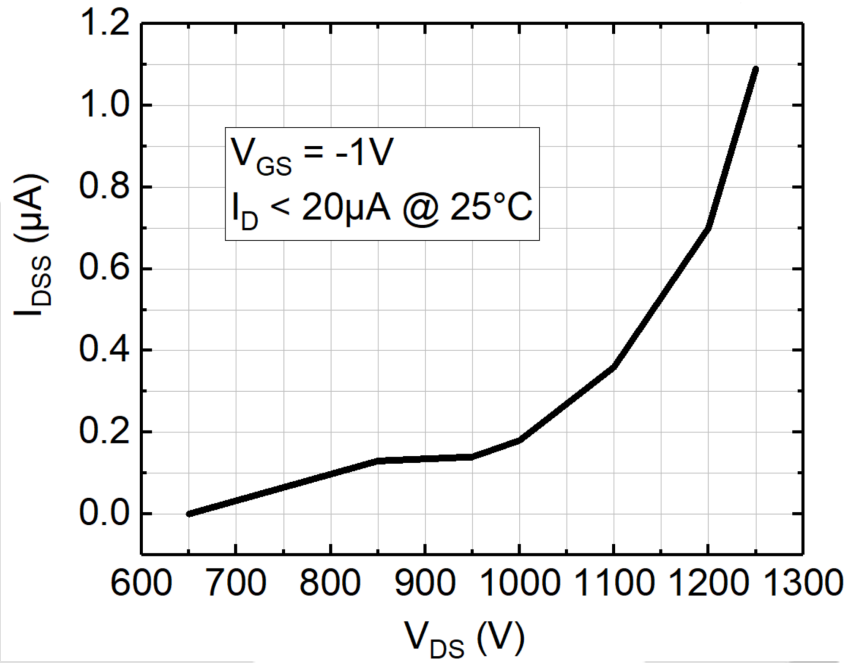
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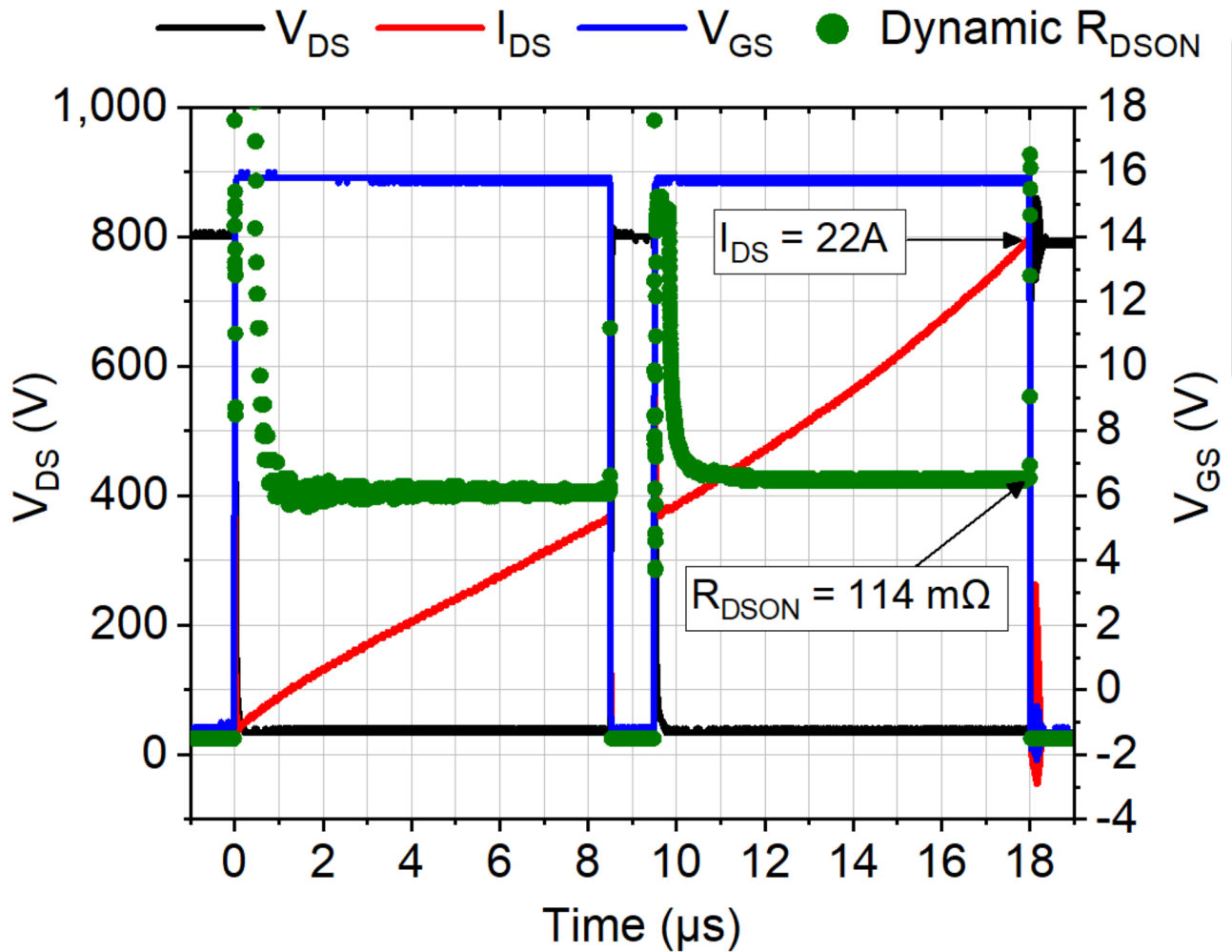
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Device Characteristics

Basic Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$V_{GS(TH)}$	Zero gate voltage drain current, $T_c = 25^\circ\text{C}$	$V_{DS} = V_{GS}$ $I_D = 3\text{mA}$	3.5	3.7		V
2	BV_{DSS}	Drain-Source breakdown voltage	$V_{GS} = 0\text{V}$ $I_D < 20\mu\text{A}$		1200		V
3	I_{DSS}	Zero gate voltage drain current, $T_c = 25^\circ\text{C}$	$V_{GS} = 0\text{V}$ $V_{DS} = 1200\text{V}$	0.5	1.0	3.0	μA
4	I_{GSS}	Gate-Source Leakage @ 25°C	$V_{GS} = 15\text{V}$ $V_{DS} = 0\text{V}$		50	70	mA
5	$R_{DS(on)}$	Static drain-source on resistance, $T_c = 25^\circ\text{C}$	$V_{GS} = 15\text{V}$	90	102	120	m Ω
Switching Performance				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$t_{D(ON)}$	Turn-on delay time	$V_{DS} = 800\text{V}$ $I_D = 9.5\text{A}$ $V_{GS} = +15\text{V}/-1\text{V}$ $R_{GON} = 2\Omega$ $R_{GOFF} = 0\Omega$		21		ns
2	t_R	Rise time			61		ns
3	$t_{D(OFF)}$	Turn-off delay time			12		ns
4	t_F	Fall time			28		ns

Electrical Performance





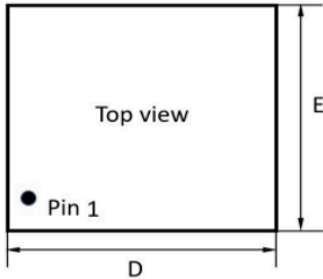
DPT @ 25°C: $V_{BUS} = 800V$, L-load = 360 μH



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Package Information

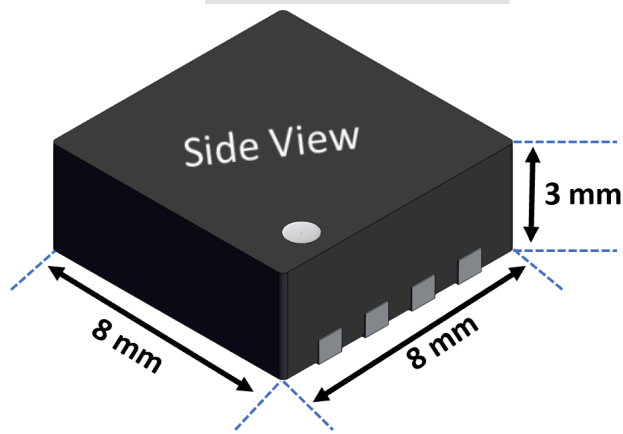
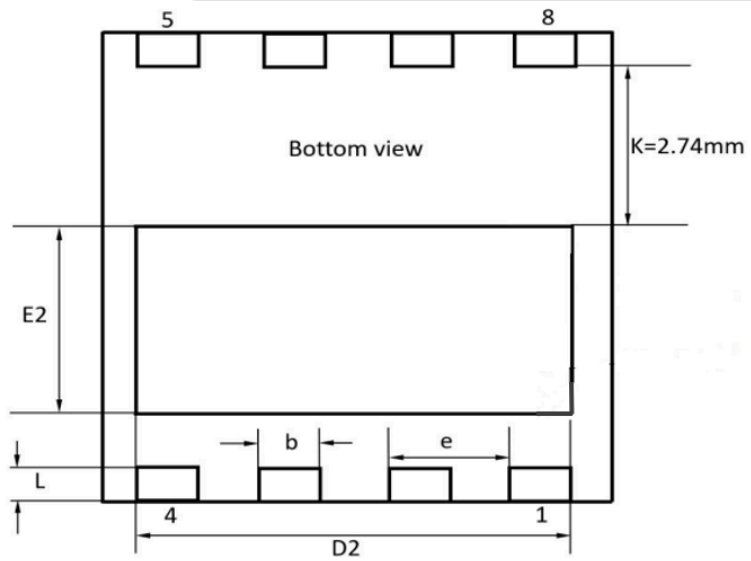


D=8; E=8; e=1.95; b=0.97;
L=0.57; D2=6.82; E2=3.19

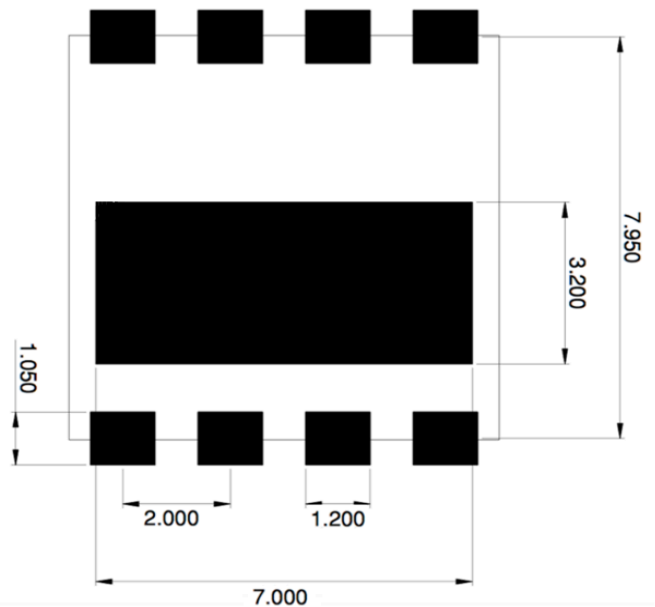
8LEAD DFN (8x8x3 mm)

Pitch 1.95mm)

**IMPORTANT: Please connect
the bottom thermal pad to
the source electrode on PCB**



Land Pattern View





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Further Information

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Data Source – Data here are based on recent tests but all parameters may not be up to date. Actual final test data from packaging production are available for selected customers upon request.