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230 -3410 LOUGHEED HWY
VANCOUVER, BC, V5M 2A4 CANADA

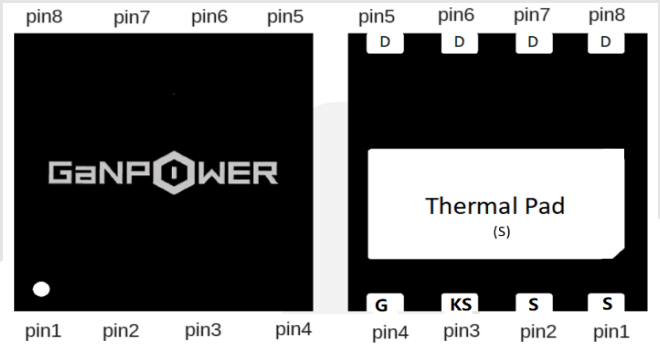
GPI90005DF88

N-channel 900V 5A GaNPower HEMT in DFN 8X8Package

Datasheet version 1.1 Preliminary

Features

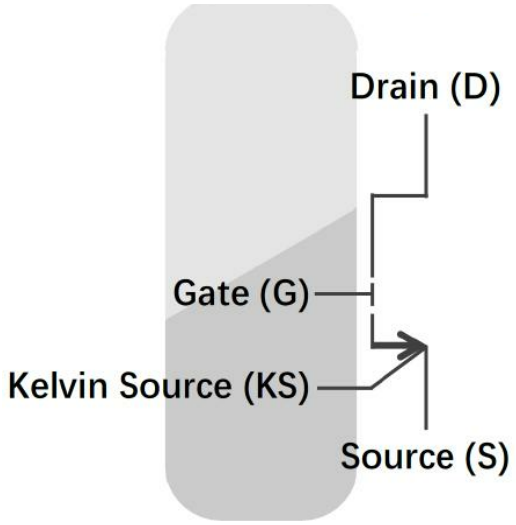
BV_{dss}	R_{dson}	I_{ds}	Q_g
900 V	235 mΩ	5 A (25 °C) 11 A (pulse)	1.6 nC



- Ultra-low $R_{DS(on)}$
- High dv/dt capability
- Extremely low input capacitance
- Zero Qrr
- Outstanding switching performance
- Low Profile

Applications

- Switching Power Applications
- Server and Telecom Power Application
- EVOBC and DC-DC Converters
- UPS, Inverters, PV



Description

These devices are N-channel 900V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology. The resulting product has extremely low on state resistance, very low input capacitance and zero reverse recovery charge making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency.

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Device Characteristics

Static Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$V_{gs(TH)}$	Gate threshold voltage	$V_{ds}=V_{gs}$, I_d=3.5mA (T_J=25 °C)	0.9	1.2	2.9	V
			$V_{ds}=V_{gs}$, I_d=3.5mA (T_J=150 °C)		1.1		V
2	BV_{dss}	Drain-Source breakdown voltage	V_{gs}=0V, I_d < 20 µA (T_J=25 °C)		900		V
3	I_{dss}	Zero gate voltage drain leakage current	V_{gs}=0V, V_{ds}= 650V TJ = 25 °C		0.7	14	µA
			V_{gs} = 0V V_{ds} = 650V TJ = 150 °C		21		µA
4	I_{gss}	Gate-Source Leakage	V_{gs} = 6V, V_{ds} = 0V		4	500	µA
5	R_{dson}	drain-source on resistance	V_{gs}=6V, I_d=1A T_J = 25 °C		235	320	mΩ
			V_{gs}=6V, I_d=1A T_J = 150 °C		580		mΩ
6	V_{sd}	Reverse conduction voltage	I_{sd}=0.1A, V_{gs}=0V	1.2	1.4	3	V
7	R_g	Gate resistance	f=25Mhz Open drain		1		Ω
Dynamic Parameters				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	C_{ISS}	Input capacitance	V_{gs} = 0 V V_{ds} = 500 V f = 100 kHz		39		pf
2	C_{OSS}	Output capacitance			11.8		pf
3	C_{RSS}	Reverse transfer capacitance			0.24		pf
4	$C_{O(er)}$	Effective output capacitance, energy related	V_{ds} = 0 - 500 V		15		pf
5	Q_g	Gate charge	V_{ds} = 500 V I_d = 2.5 A V_{gs} = 6 V		1.6		nC
6	Q_{gs}	Gate to source charge			0.30		nC
7	Q_{gd}	Gate to drain charge			0.38		nC
8	Q_{OSS}	Output Charge	V_{ds} = 0 - 500 V		10		nC
9	Q_{rr}	Reverse recovery charge			0		nC

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Switching Performance				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	td(on)	Turn-on delay time	V_{ds} = 600 V Id = 1.2 A R_g= 22/2 Ω V_{gs} = -3/6 V		40		ns
2	tr	Rise time			20		ns
3	td(off)	Turn-off delay time			39		ns
4	tf	Fall time			90		ns

Absolute Max. Ratings

	Symbols	Parameters	Value	Unit
1	$V_{DS\text{-}max}$	Breakdown voltage transient @ Tcase=25°C	900	V
2	$V_{DS\text{-}max}$	Breakdown voltage transient @ Tcase=125°C	900	V
3	$V_{GS\text{-}max}$	Gate to source max. voltage @ Tcase=25°C	-12 to +7.5	V
4	$I_{ds\text{-}max}$	Drain to source DC continuous current @ Tcase=25°C	5	A
5	$I_{ds\text{-}max}$	Drain to source pulse current @ Tcase=25°C, pulse width 10 µs, V_{GS} = 6 V	11	A
6	$I_{ds\text{-}max}$	Drain to source DC current @ Tcase=100°C	5	A
7	$dv/dt_{\text{-}max}$	Drain to source voltage slew rate	150	V/ns
8	$T_{J\text{-}max}$	Max junction temperature	150	°C
9	$T_{S\text{-}storage}$	Storage temperature	-55 to 150	°C

Thermal and Soldering Characteristics (Typical)

	Symbols	Parameters	Value	Unit
1	R_{thJC}	Thermal resistance (junction to case)	1.4	°C /W
2	R_{thJA}	Thermal resistance (junction to ambient)	62	°C /W
3	T_{solder}	Reflow soldering temperature	260	°C

Ordering

Order Code	Package Type	Packaging Method	Qty
GPI90005DF88	DFN8x8		

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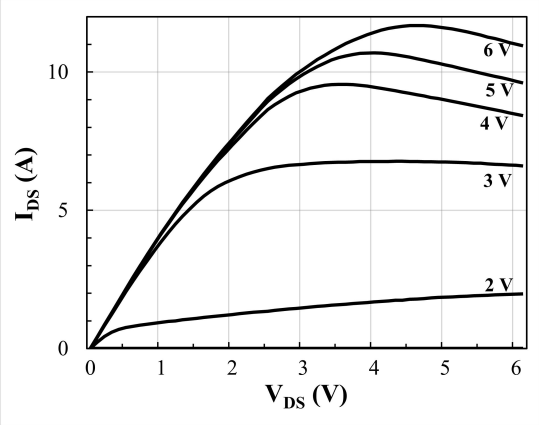
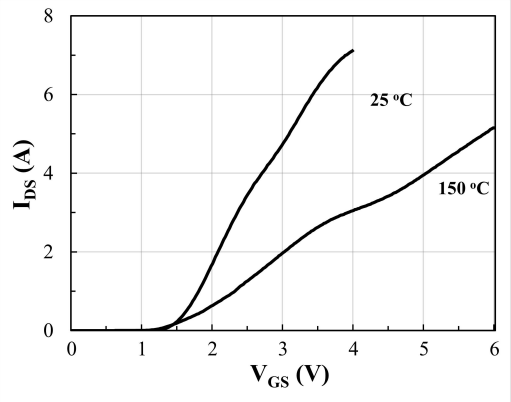
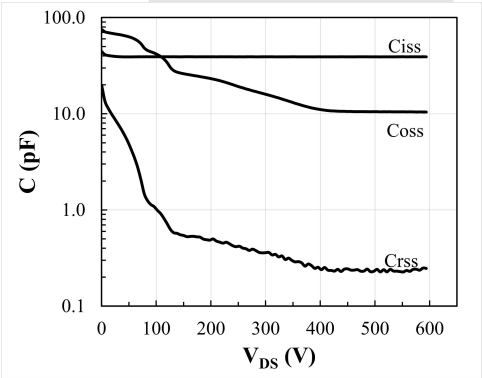
Electrical Performance



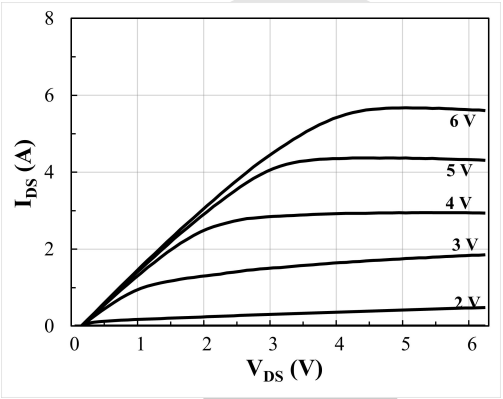
I_{DS} vs. V_{DS} @ T_j = 25 °C



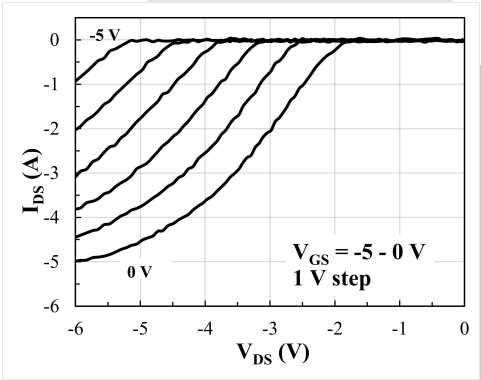
I_{DS} vs. V_{GS} @ T_j = 25 °C and 150 °C



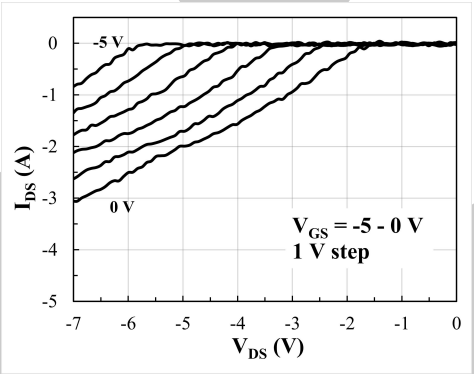
Capacitance vs. V_{ds} Curve @ T_j=25 °C



I_{DS} vs. V_{DS} @ T_j = 150 °C



I_{sd} vs. V_{sd} reverse conduction curve @ T_j = 25 °C



I_{sd} vs. V_{sd} reverse conduction curve @ T_j = 150°C

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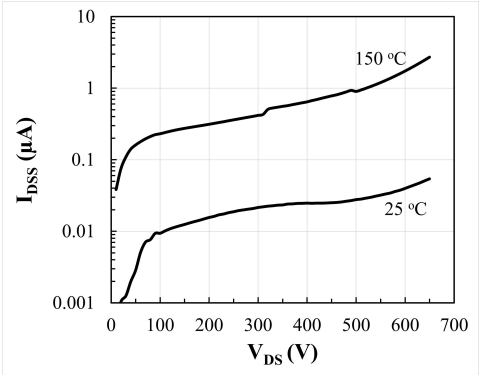
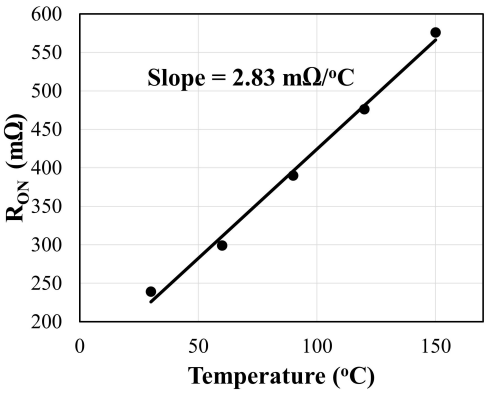
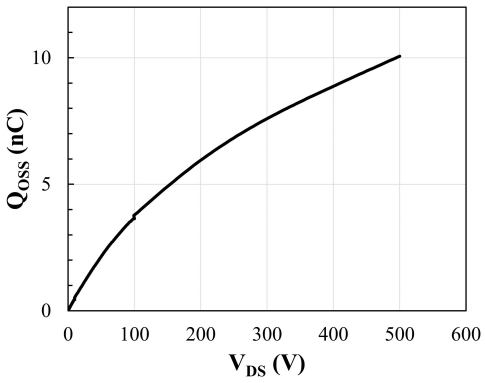


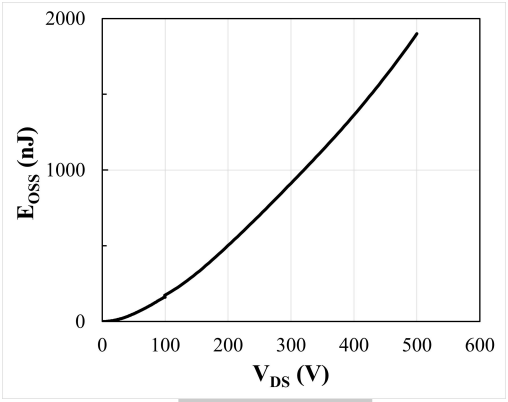
Typical off-state drain leakage current I_{DSS} vs. V_{DS} @ T_J = 25 °C and 150 °C



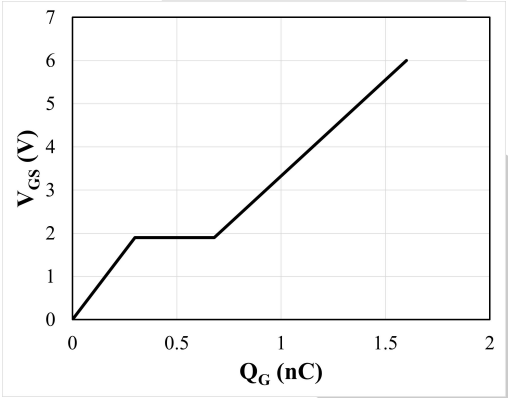
On-state resistance vs. T_J @ I_D = 2.5 A, V_{GS} = 6V



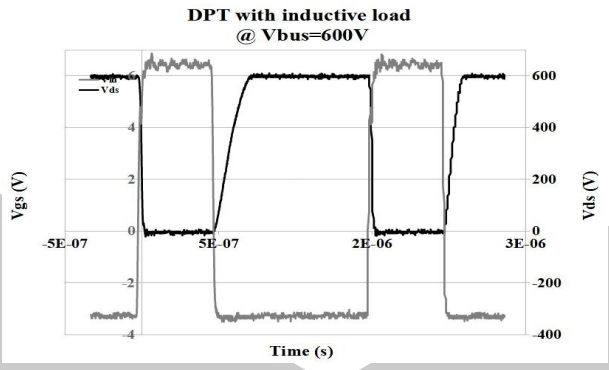
Output charge Q_{OSS} vs. V_{DS}



Stored Energy Characteristic E_{OSS} vs. V_{DS}



Gate charge V_{GS} vs. Q_G



DPT waveform, 1st off@1.2A, 2nd off@2.4A

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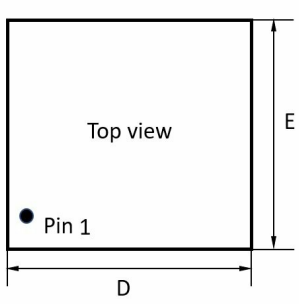
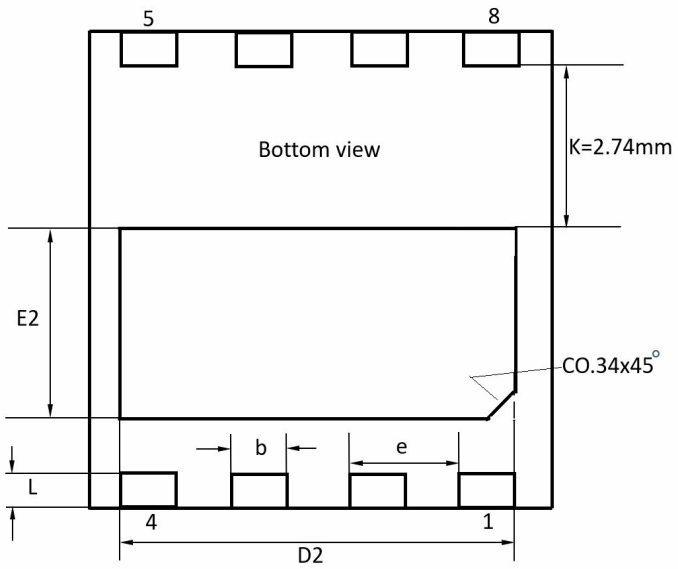
Package Information

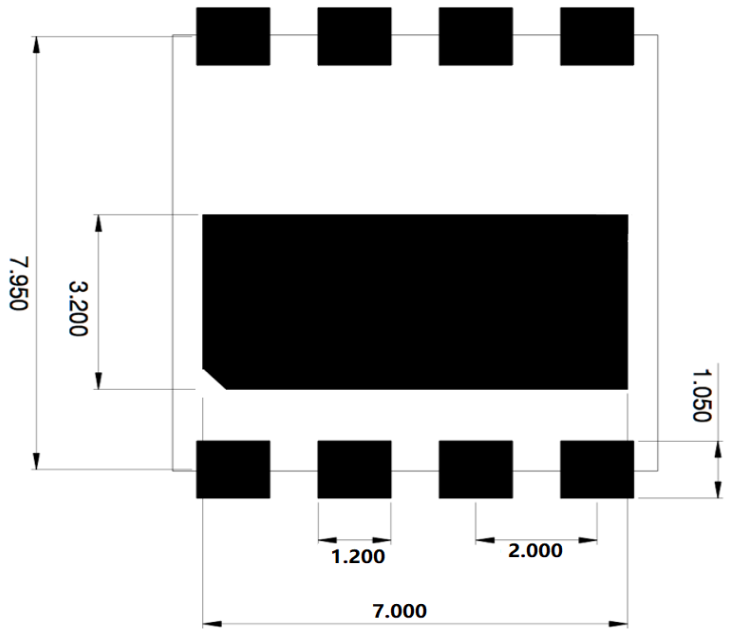


D=8; E=8; e=1.95; b=0.97; L=0.57; D2=6.82; E2=3.19

8LEAD DFN (8x8x0.75mm, Pitch 1.95mm)
IMPORTANT: Please connect the bottom thermal pad to the source electrode on PCB



Land Pattern View



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Further Information

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Data Source– Data here are based on recent tests but all parameters may not be up to date. Actual final test data from packaging production are available for selected customers upon request.