

GPI65060DFN

N-channel 650 V 60 A GaN Power HEMT in DFN8x8 package

Datasheet version: 2.9

Features

BV_{dss}	R_{dson}	I_{ds}	Q_g
650 V	25 mΩ	60 A	16 nC

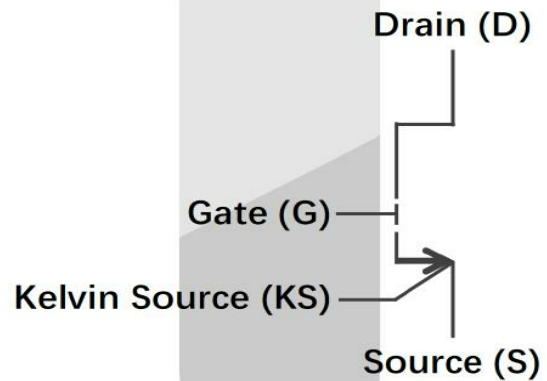
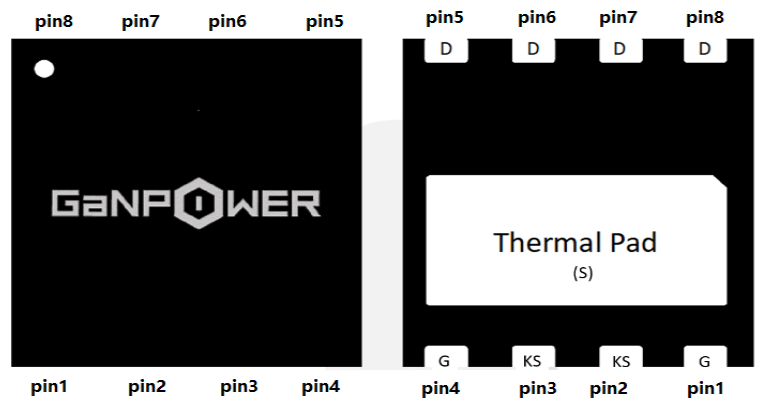
- Ultra-low $R_{DS(on)}$
- High dv/dt capability
- Extremely low input capacitance
- Zero Q_{rr}
- Outstanding switching performance
- Low Profile

Applications

- Switching Power Applications
- Server and Telecom Power Applications
- EV OBC and DC-DC Converters

Description

These devices are N-channel 650 V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology. The resulting product has extremely low on state resistance, very low input capacitance and zero reverse recovery charge making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency.





GaNPower International Inc.

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230 -3410 LOUGHEED HWY
VANCOUVER, BC, V5M 2A4 CANADA

Device Characteristics

Static Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$V_{gs(TH)}$	Gate threshold voltage	$V_{ds}=V_{gs}$ $I_d=42mA$	0.9	1.2	2.9	V
2	BV_{dss}	Drain-Source breakdown voltage	$V_{gs}=0V$ $I_d<100\ \mu A$		650		V
3	I_{dss}	Zero gate voltage drain current, $T_c = 25^\circ C$	$V_{gs}=0V$ $V_{ds}=650V$		0.6	100	μA
4	I_{gss}	Gate-Source Leakage	$V_{gs} = 6V$ $V_{ds} = 0V$		0.347	6	mA
5	R_{dson}	Static drain-source on resistance, $T_c = 25^\circ C$	$V_{gs}=6V$ $I_d=12A$		25	30	m Ω
6	V_{sd}	Reverse conduction voltage	$I_{sd}=1.6A$ $V_{gs}=0V$	1.5	1.75	3.0	V
7	R_g	Gate resistance	F=25MHz Open drain		2.18		Ω
Dynamic Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	C_{iss}	Input capacitance	$V_{gs}=0V$ $V_{ds}=400V$ f=1MHz		420		pf
	C_{oss}	Output capacitance			143		pf
	C_{rss}	Reverse transfer capacitance			6		pf
3	Q_g	Gate charge	$V_{ds}=400V$ $I_d=7.5A$ $V_{gs}=6V$		16.1		nC
	Q_{gs}	Gate to source charge			1.1		nC
	Q_{gd}	Gate to drain charge			1.8		nC
2	Q_{rr}	Reverse recovery charge			0		nC
Switching Performance				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$t_{d(on)}$	Turn-on delay time	$V_{ds}=400V$ $I_d=2.5A$ $R_g=10\Omega$ $V_{gs}=6V$		9		ns
2	t_r	Rise time			17		ns
3	$t_{d(off)}$	Turn-off delay time			26		ns
4	t_f	Fall time			17		ns



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Absolute Max. Ratings

	Symbols	Parameters	Value	Unit
1	V_{DS-max}	Breakdown voltage transient @ $T_{case}=25^{\circ}C$	800	V
2	V_{GS-max}	Gate to source max. transient voltage @ $T_{case}=25^{\circ}C$	-12 to +7.5	V
3	I_{ds-max}	Drain to source DC current @ $T_{case}=25^{\circ}C$	60	A
4	I_{ds-max}	Drain to source DC current @ $T_{case}=100^{\circ}C$	50	A
5	dv/dt_{-max}	Drain to source voltage slew rate	200	V/ns
6	T_J-max	Max junction temperature	150	$^{\circ}C$
7	$T_S-storage$	Storage temperature	-55 to 150	$^{\circ}C$

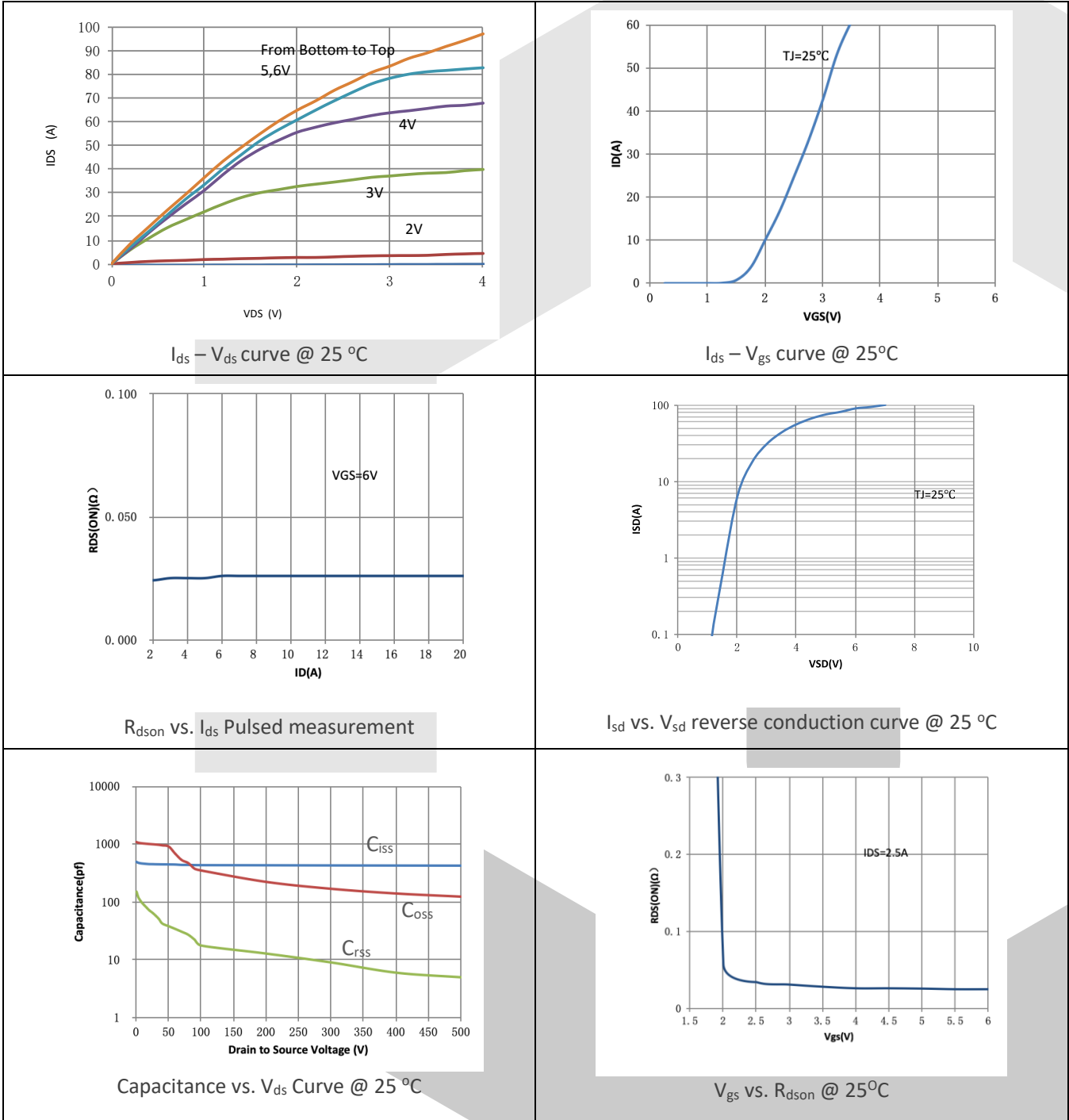
Thermal and Soldering Characteristics (Typical)

	Symbols	Parameters	Value	Unit
1	R_{thJC}	Thermal resistance (junction to case)	0.6	$^{\circ}C/W$
2	R_{thJA}	Thermal resistance (junction to ambient)	62	$^{\circ}C/W$
2	T_{solder}	Reflow soldering temperature	260	$^{\circ}C$

Ordering

Order Code	Package Type	Packaging Method	Qty
GPI65060DFN	DFN 8x8	QFN/DFN-Tray	100

Electrical Performance

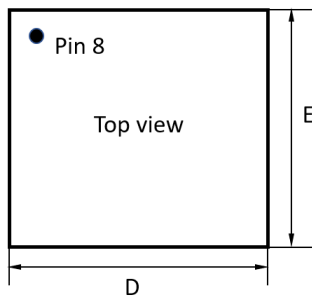




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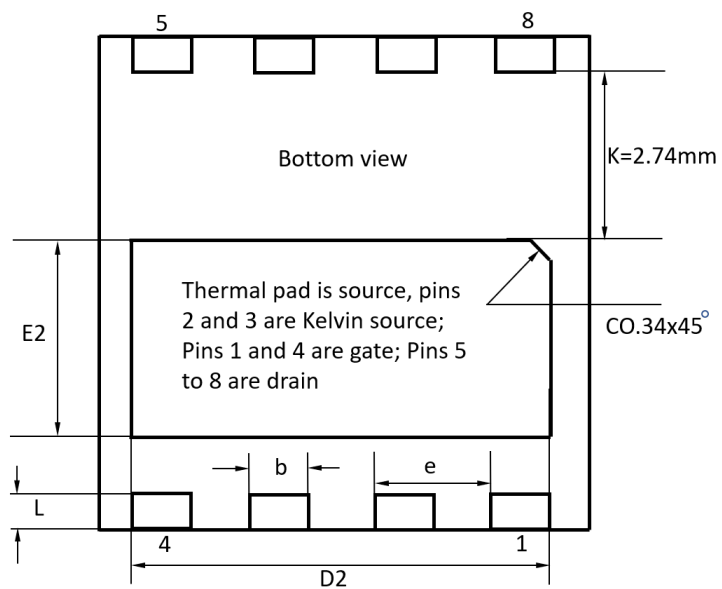
Package Information



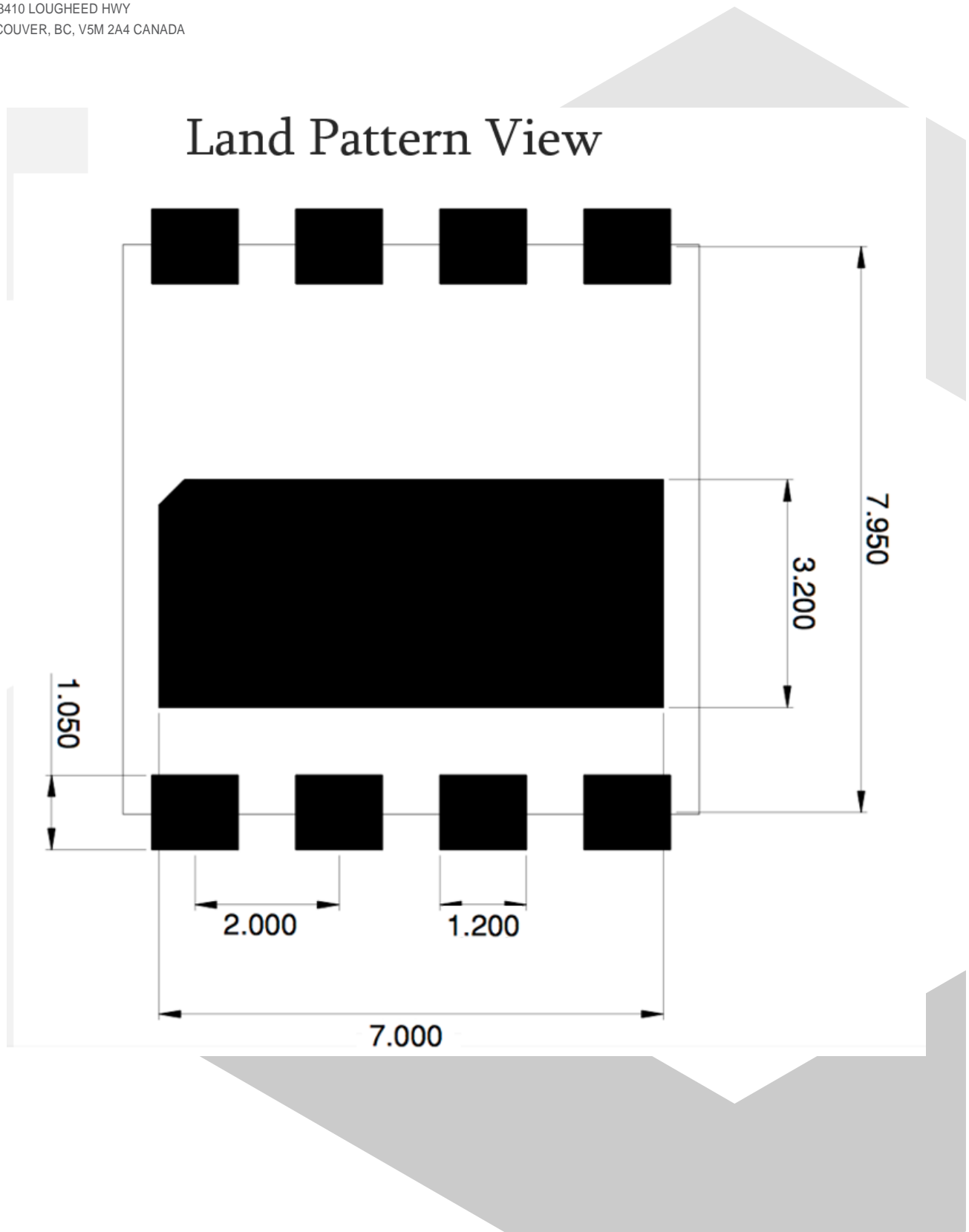
D=8; E=8; e=1.95; b=0.97;
L=0.57; D2=6.82; E2=3.19

8LEAD DFN (8x8x0.75mm,
Pitch 1.95mm)

**IMPORTANT: Please connect
the bottom thermal pad to
the source electrode on PCB**



Land Pattern View





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Further Information

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Data Source– Data here are based on recent tests but all parameters may not be up to date. Actual final test data from packaging production are available for selected customers upon request.