GaNPower International Inc.

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GPI65005DF68

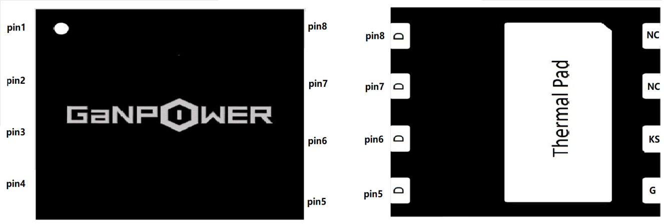
N-channel 650V 5A GaNPower HEMT in DFN **6X8** Package

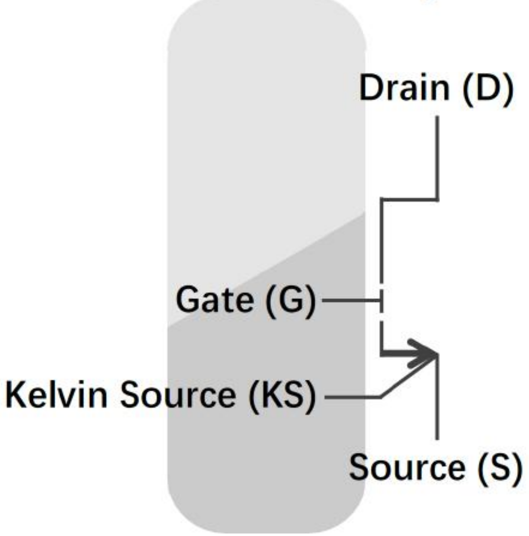
Datasheet version 2.8

Features

BV_{dss}	R_{dson}	I_{ds}	Q_g
650 V	235 mΩ	5A	1.6 nC

- Ultra-low $R_{DS(on)}$
- High dv/dt capability
- Extremely low input capacitance
- Zero Qrr
- Outstanding switching performance
- Low Profile





Applications

- Switching Power Applications
- Server and Telecom Power Application
- EVOBC and DC-DC Converters
- UPS, Inverters, PV

Description

These devices are N-channel 650 V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology. The resulting product has extremely low on state resistance, very low input capacitance and zero reverse recovery charge making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency.

Device Characteristics

Static Parameters				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	$V_{gs(TH)}$	Gate threshold voltage	$V_{ds}=V_{gs}$, $I_d=3.5mA$ ($T_J=25$ °C)	0.9	1.25	1.7	V
			$V_{ds}=V_{gs}$, $I_d=3.5mA$ ($T_J=150$ °C)		1.15		V
2	BV_{dss}	Drain-Source breakdown voltage	$V_{gs}=0V$, $I_d < 1$ µA ($T_J=25$ °C)		650	800	V
3	I_{dss}	Zero gate voltage drain leakage current	$V_{gs}=0V$, $V_{ds}= 650V$ TJ = 25 °C		0.1	1	µA
			$V_{gs} = 0V$ $V_{ds} = 650V$ TJ = 150 °C		3		µA
4	I_{gss}	Gate-Source Leakage	$V_{gs} = 6V$, $V_{ds} = 0V$		13	50	µA
5	R_{dson}	drain-source on resistance	$V_{gs}=6V$, $I_d=1.25A$ TJ = 25 °C		235	300	mΩ
			Vgs=6V, Id=1.25A TJ = 150 °C		580		mΩ
6	V_{sd}	Reverse conduction voltage	$I_{sd}=1A$, $V_{gs}=0V$	1.4	2.2	3	V
7	R_g	Gate resistance	f=25Mhz Open drain		1		Ω
Dynamic Parameters				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	C_{ISS}	Input capacitance	$V_{gs} = 0$ V $V_{ds} = 500$ V f = 100 kHz		39		pf
2	C_{OSS}	Output capacitance			11.8		pf
3	C_{RSS}	Reverse transfer capacitance			0.24		pf
4	$C_{O(er)}$	Effective output capacitance, energy related	$V_{ds} = 0 - 500$ V		15		pf
5	Q_g	Gate charge	$V_{ds} = 500$ V $I_d = 2.5$ A $V_{gs} = 6$ V		1.6		nC
6	Q_{gs}	Gate to source charge			0.30		nC
7	Q_{gd}	Gate to drain charge			0.38		nC
8	Q_{OSS}	Output Charge	$V_{ds} = 0 - 500$ V		10		nC
9	Q_{rr}	Reverse recovery charge			0		nC

Switching Performance				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	td(on)	Turn-on delay time	V_{ds} = 500 V Id = 1.25 A R_g= 22/2 Ω V_{gs} = -3/6 V		5		ns
2	tr	Rise time			10		ns
3	td(off)	Turn-off delay time			16		ns
4	tf	Fall time			11		ns

Absolute Max. Ratings

	Symbols	**Parameters**	**Value**	**Unit**
1	$V_{DS\text{-}max}$	Breakdown voltage transient @ Tcase=25°C	800	V
2	$V_{DS\text{-}max}$	Breakdown voltage transient @ Tcase=125°C	650	V
3	$V_{GS\text{-}max}$	Gate to source max. voltage @ Tcase=25°C	-12 to +7.5	V
4	$I_{ds\text{-}max}$	Drain to source DC current @ Tcase=25 °C	5	A
5	$I_{ds\text{-}max}$	Drain to source pulse current @ Tcase=25°C, pulse width 10 µs, V_{GS} = 6 V	11	A
6	$I_{ds\text{-}max}$	Drain to source pulse current @ Tcase=125°C	5	A
7	$dv/dt_{\text{-}max}$	Drain to source voltage slew rate	150	V/ns
8	$T_{J\text{-}max}$	Max junction temperature	150	°C
9	$T_{S\text{-}storage}$	Storage temperature	-55 to 150	°C

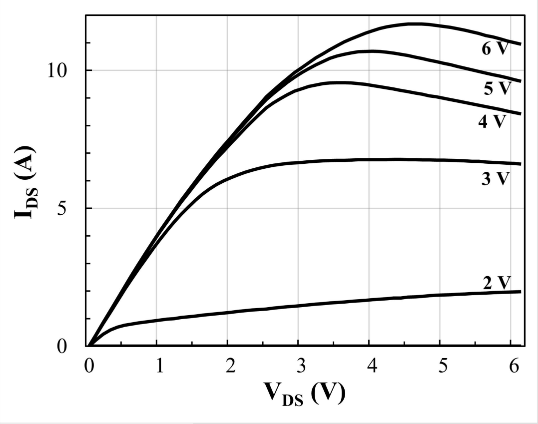
Thermal and Soldering Characteristics (Typical)

	Symbols	**Parameters**	**Value**	**Unit**
1	R_{thJC}	Thermal resistance (junction to case)	1.4	°C /W
2	R_{thJA}	Thermal resistance (junction to ambient)	62	°C /W
3	T_{solder}	Reflow soldering temperature	260	°C

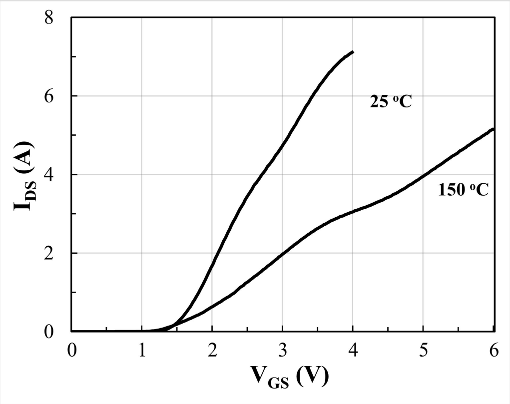
Ordering

Order Code	**Package Type**	**Packaging Method**	**Qty**
GPI65005DF	DFN5x6		

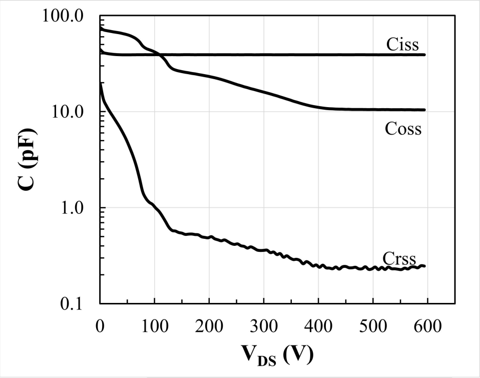
Electrical Performance



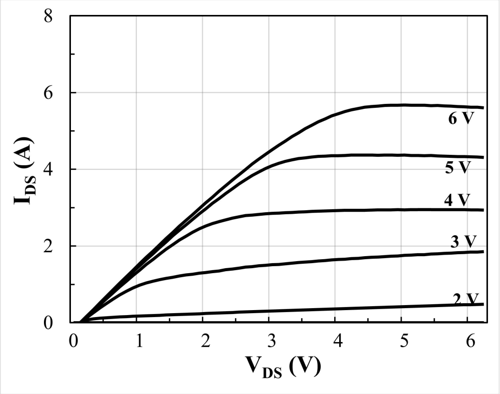
I_{DS} vs. V_{DS} @ T_j = 25 °C



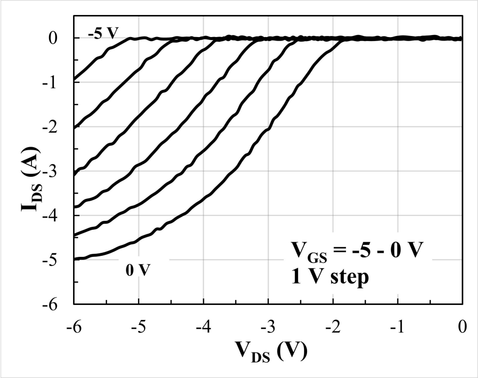
I_{DS} vs. V_{GS} @ T_j = 25 °C and 150 °C



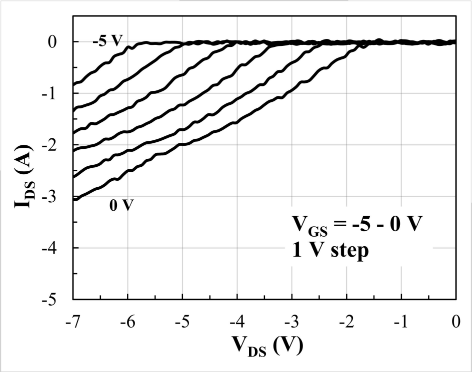
Capacitance vs. V_{ds} Curve @ T_j =25 °C



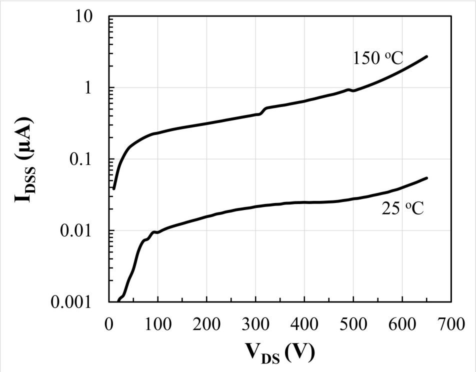
I_{DS} vs. V_{DS} @ T_j = 150 °C



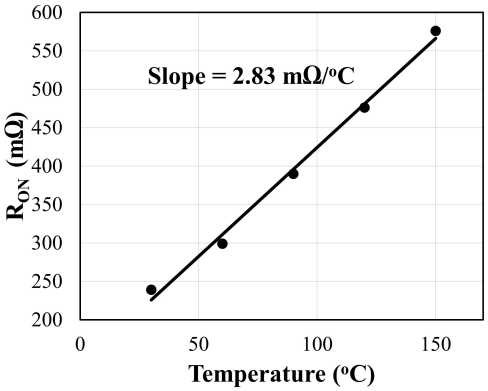
I_{sd} vs. V_{sd} reverse conduction curve @ T_j = 25 °C



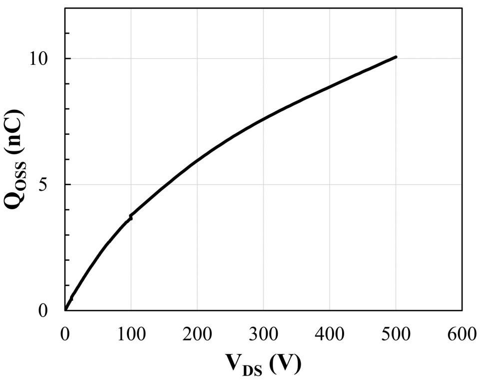
I_{sd} vs. V_{sd} reverse conduction curve @ T_j = 150°C



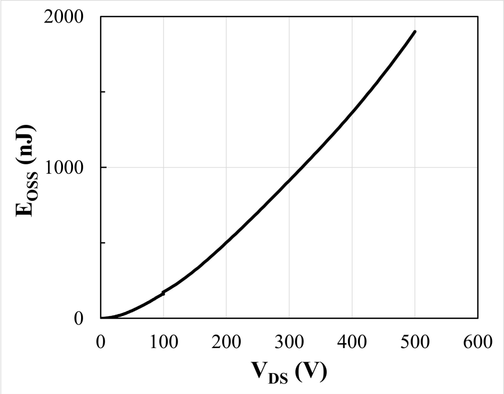
Typical off-state drain leakage current I_{DSS} vs. V_{DS} @ T_J = 25 °C and 150 °C



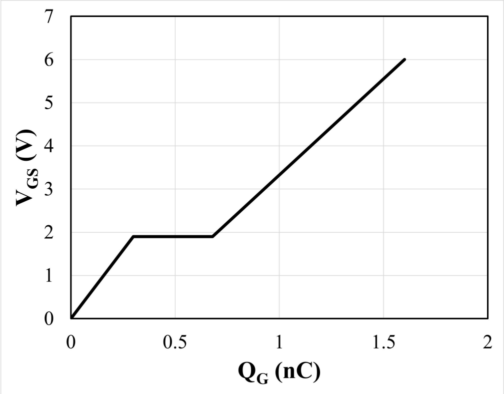
On-state resistance vs. T_J @ I_D = 2.5 A, V_{GS} = 6V



Output charge Q_{OSS} vs. V_{DS}

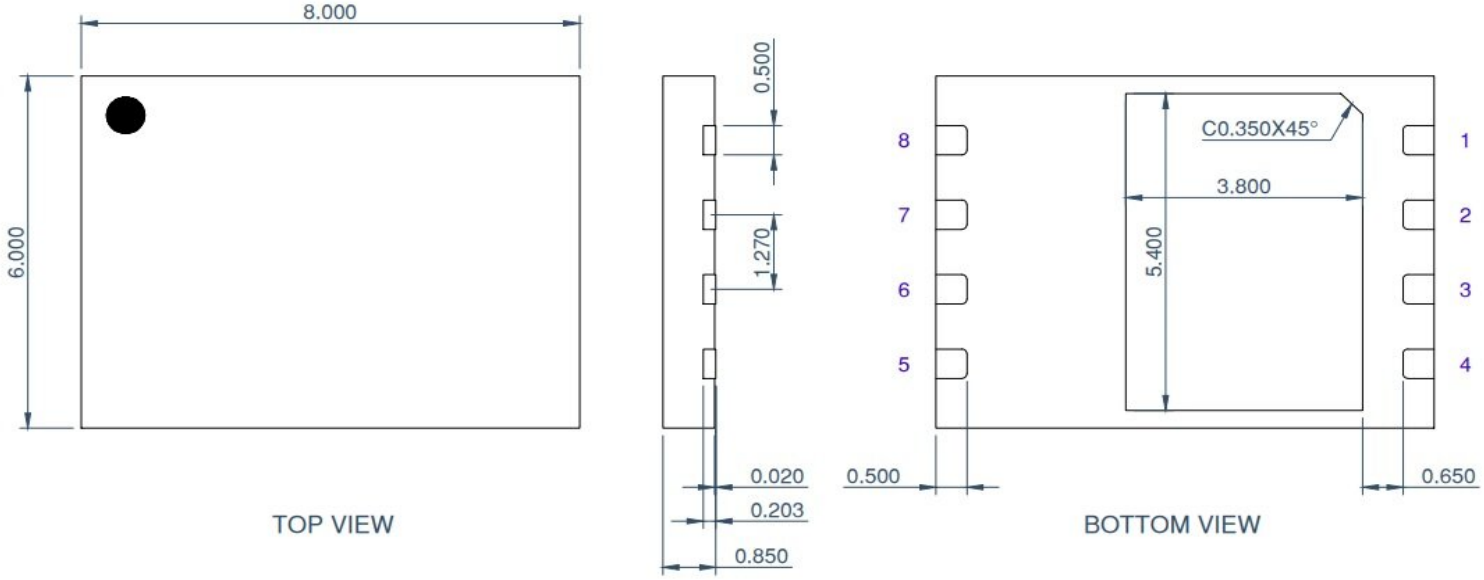


Stored Energy Characteristic E_{OSS} vs. V_{DS}



Gate charge V_{GS} vs. Q_G

Package Information



PKG nom. thickness : 0.85mm (Y type)
LF THICKNESS : 0.203±0.008 THK

GaN HEMT Frequently Asked Questions

1	Q: Can we do pin to pin switch for silicon MOSFET or IGBT? A: The short answer is no. GaN HEMT power devices are far superior than the best silicon devices such as super junction MOSFETs. However, due to different requirements of gate driving voltage and extremely high dv/dt slew rate, special drivers and optimized PCB layouts are recommended to minimize the impact from circuit parasitics.
2	Q: How do GaN power devices compare with SiC? A: Currently GaN power HEMT devices are most suitable for low to medium voltage (⩽1200V) and power (<20KW) applications. GaN is the ideal choice for high frequency applications. SiC devices are better choice for high voltage and high-power applications (>20KW).
3	Q: Do we need to parallel an FRD for applications such as inverters? A: GaN devices are different from silicon MOSFET or IGBT in that they have no inherent PN junction diodes that cause reverse recovery issue. User do not need to parallel an FRD for the purpose of suppressing the body diode reverse recovery effect, since GaN HEMT can operate in both first and third quadrants. However, care should be taken for the dead time power loss since the Vsd voltage of GaN HEMT is usually close to 2V. This is especially true when a negative gate voltage is applied.
4	Q: Can we parallel GaN HEMT devices? A: Yes, GaN HEMT is ideal for paralleling, due to the positive temperature coefficient of $R_{ds,on}$. Hence, paralleling GaN HEMT devices are encouraged.