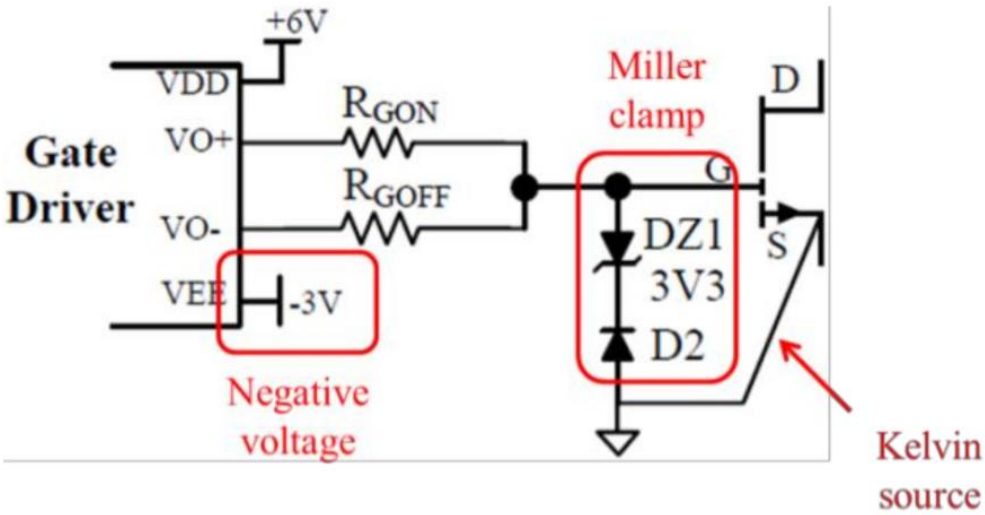
GaNPower half-bridge evaluation board –Optocoupler driving (Ver.1)

- **Overview**
- **Half-bridge optocoupler driving**
- **Double pulse test**

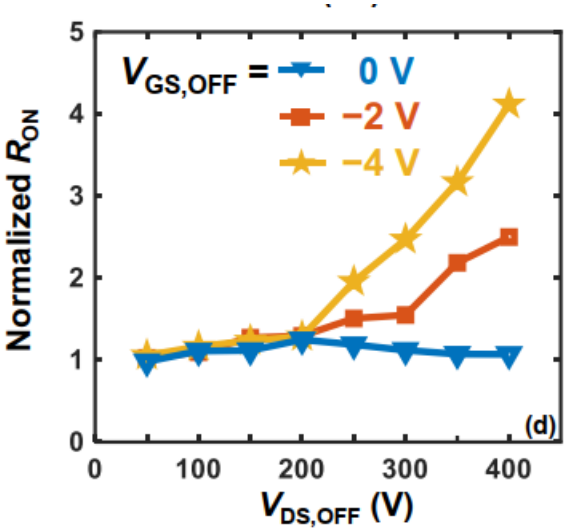
Jan. 2022

Introduction of GaNFET driving

It is generally recognized that driving discrete EMODE GaNFET requires a number of techniques, including negative voltage, differential on/off gate resistance, Miller clamping and Kelvin source connection for the driving loop. [https://doi.org/10.3390/mi12010065]



It was also found that the negative biasing affects the dynamic resistance of the GaNFET [DOI 10.1109/TPEL.2021.3130767]



R_{ON} of *p*-GaN gate Dynamic HEMTs with different drain bias stresses from 50 V to 400 V and $V_{GS,OFF}$ of (a) 0 V, (b) –2 V, and (c) –4 V, respectively. The load current I_{load} is 8 A, and ON-state V_{GS} is 6 V.

Jan. 2022

Introduction of GaNFET driving

GaNPower's half-bridge evaluation board HBEVB-opt uses separate isolated auxiliary DC power supply and separate optically coupled driving PWM signal. It enables users of GaNFET to investigate the optimal driving parameters without the worry of bootstrap circuit interfering with high side driving.

It is also offers the flexibility in controlling negative biasing and on/off gate resistance control. It can easily be converted to double pulse testing circuit for turn-on/off characteristics of hard switching.

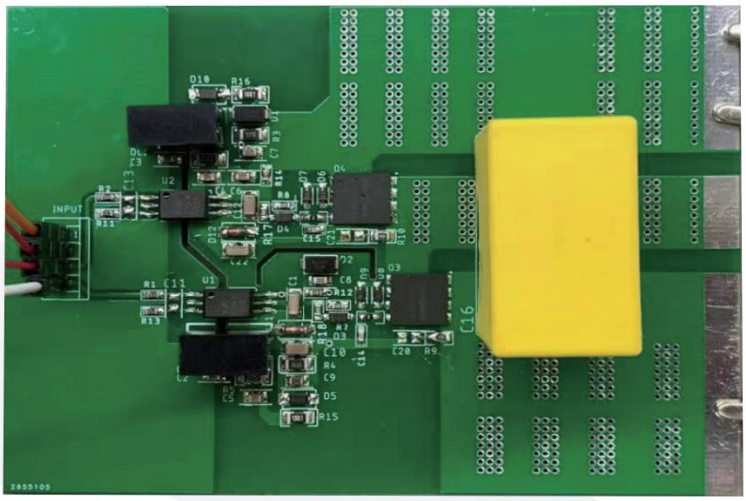
Jan. 2022

GaNPOWER

Half Bridge Evalutation Board

Overview

The Integrated Circuits Half Bridge Driver-Switch is a demonstration board containing two 650V, 30A GaN FETs configured in a half bridge configuration.

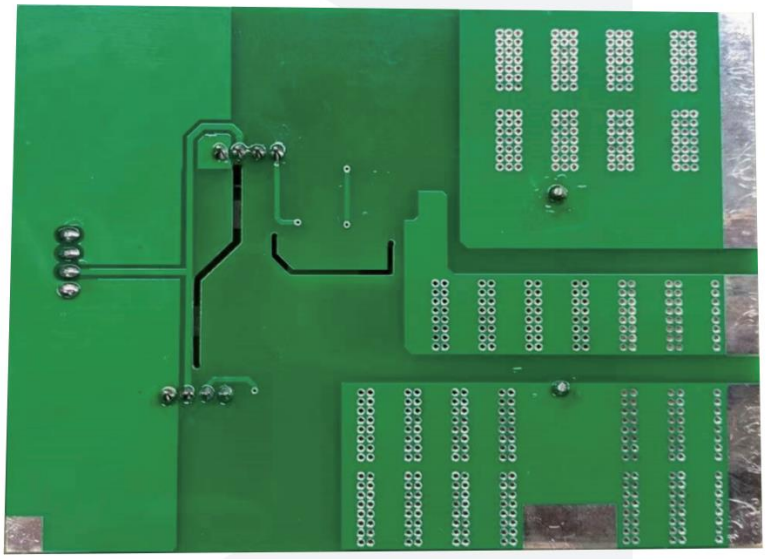


Top side

GPI65030DFN GaN Driver Description

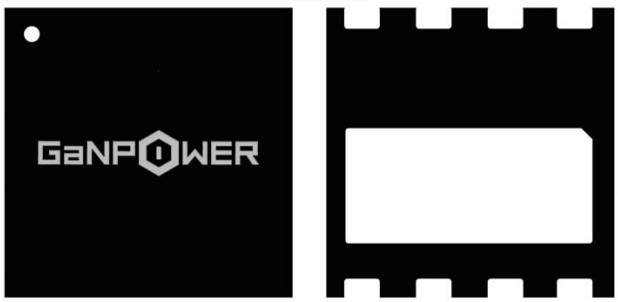
These devices are N-channel 650 V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology.

The resulting product has extremely low on state resistance, very low input capacitance and zero reverse recovery charge making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency.



Bottom side

Although the EVB is tested for GPI65030DFN, This evaluation board can be adapted for other 650/1200V GaNFET based on p-GaN Emode technology. The EVB is designed with maximum bus voltage of 1200V in mind.



07-01-2022 Ver 1.0

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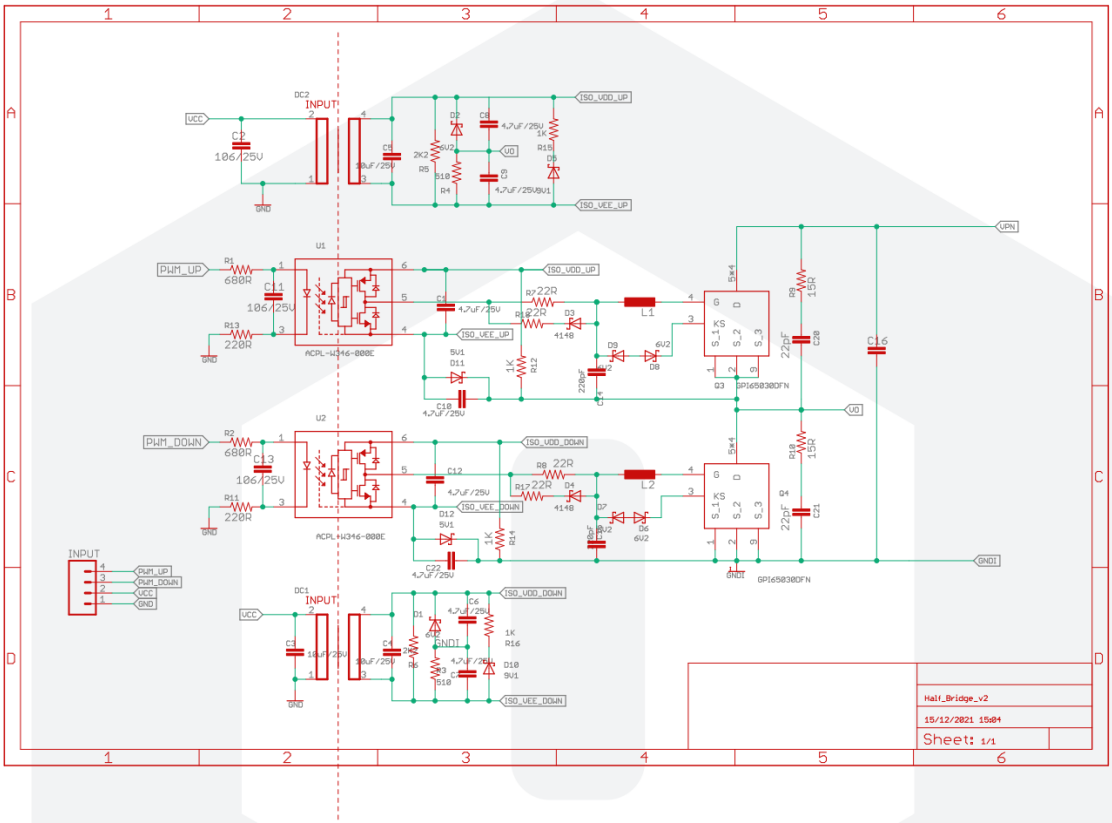
Schematic



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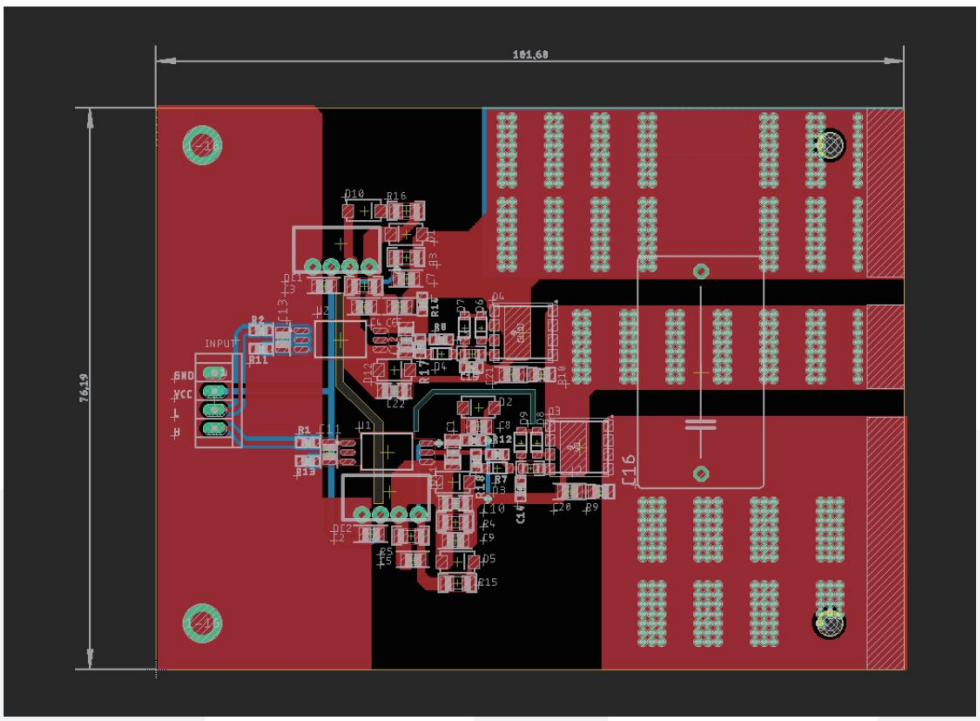
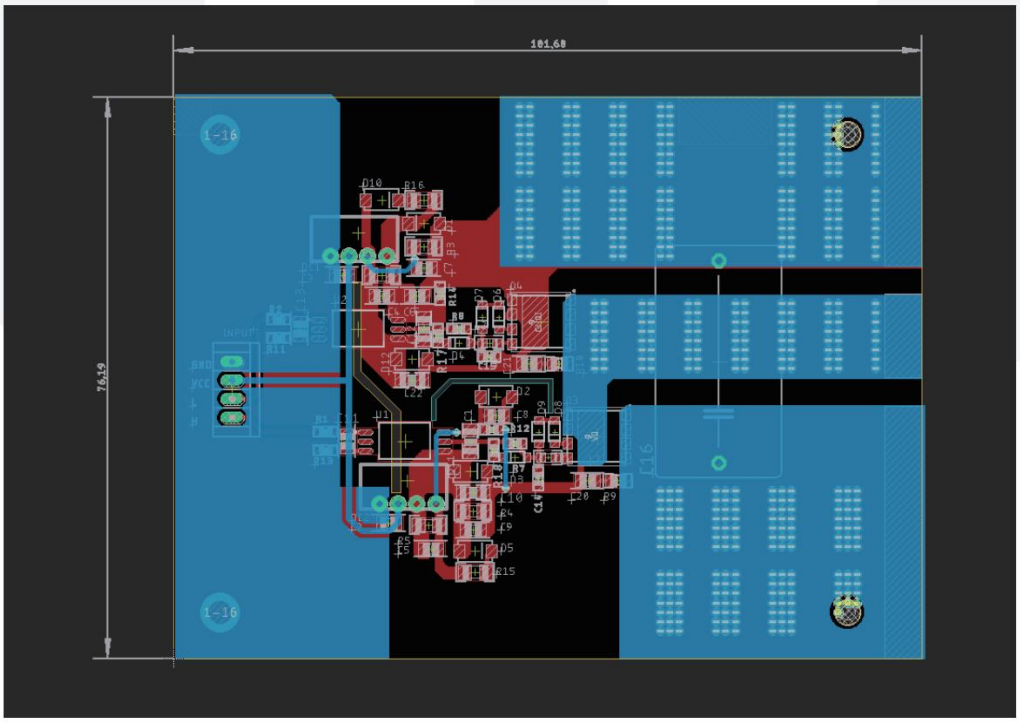
Hardware .....

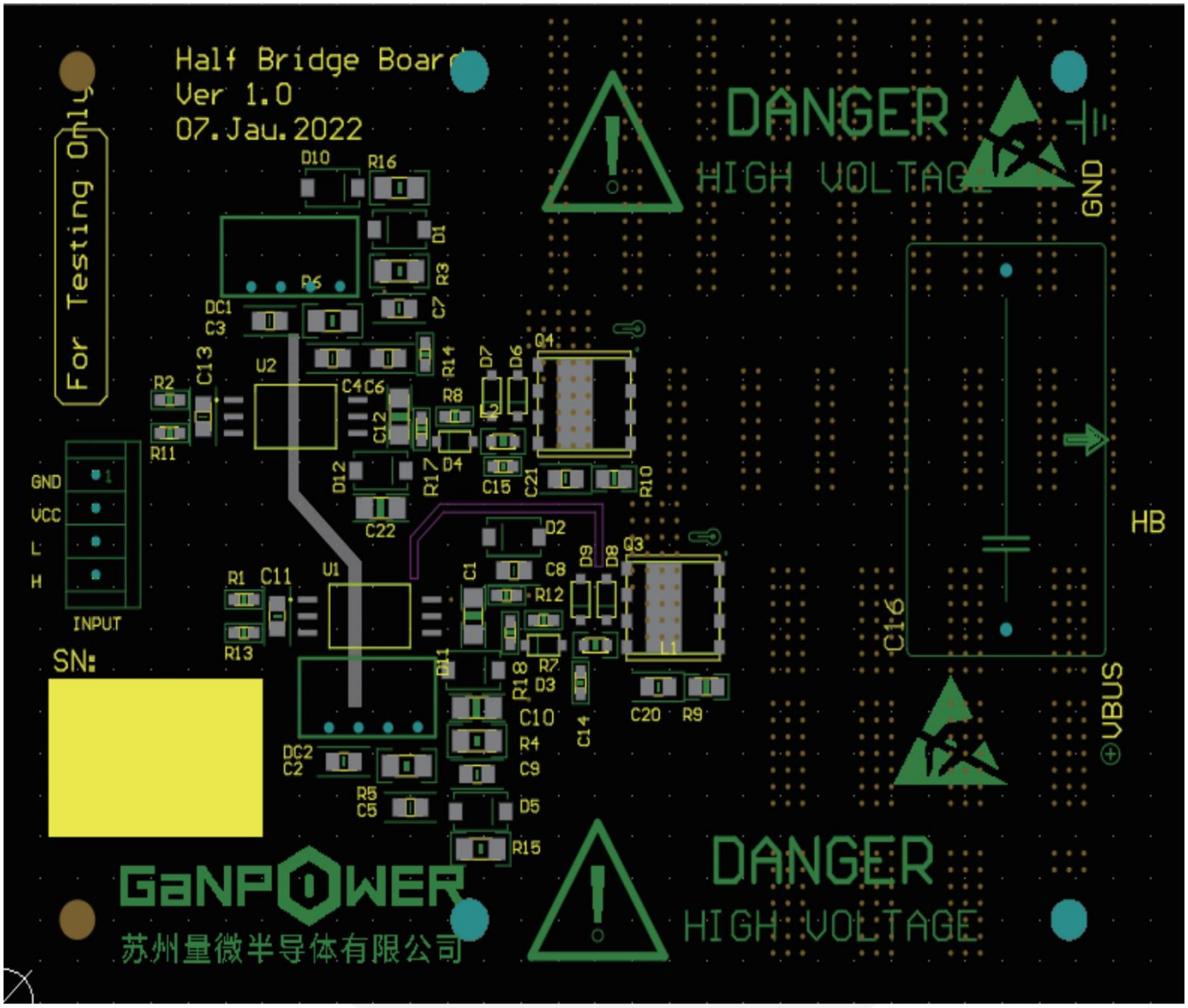
Top side



Bottom side



Demo 板结构示意


Half Bridge Board
Ver 1.0
07.Jau.2022
For Testing Only
DANGER
HIGH VOLTAGE
GND
HB
VBUS
INPUT
SN:
GND
VCC
L
H
GaNPOWER
苏州量微半导体有限公司
DANGER
HIGH VOLTAGE

Half Bridge I/C Connections

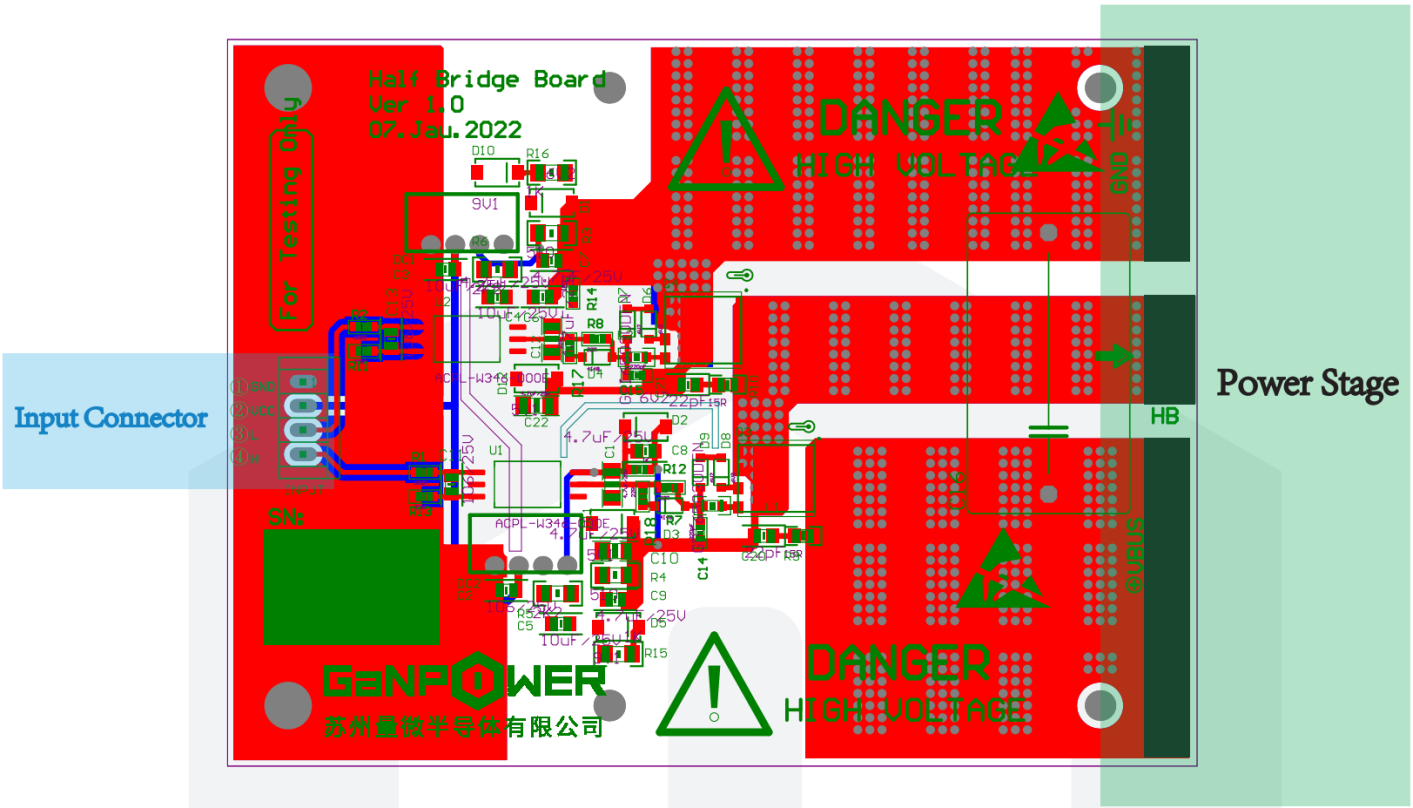
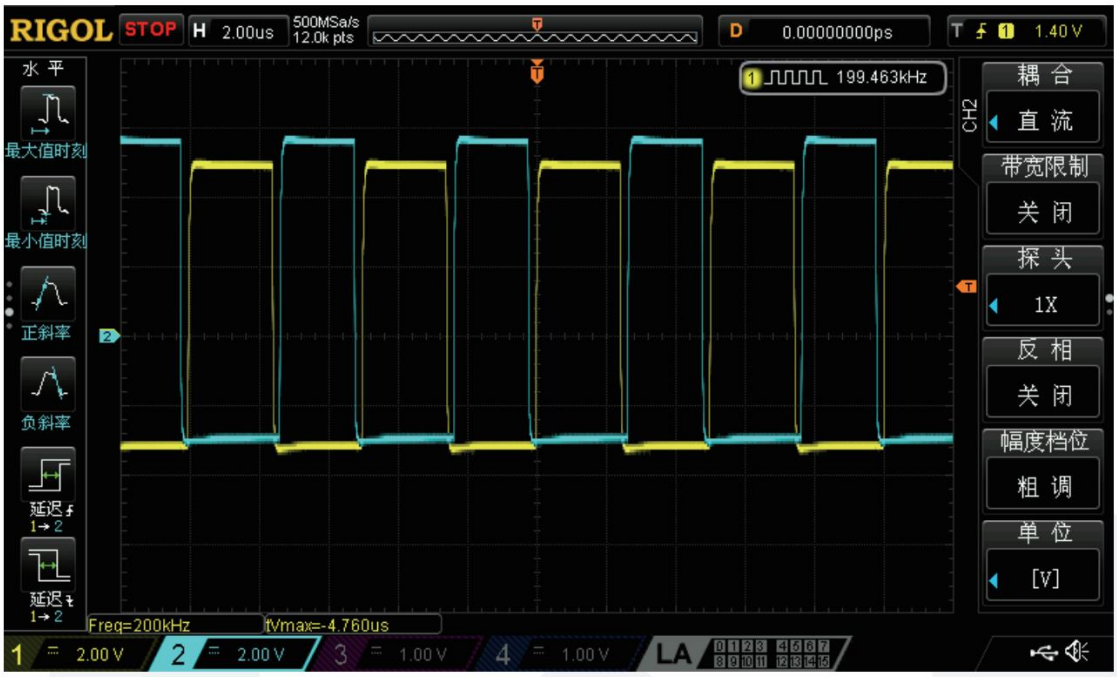


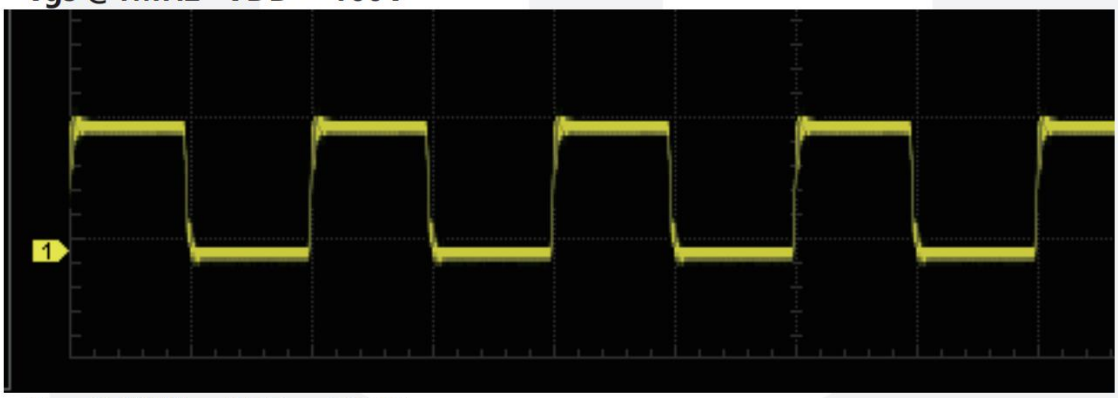
Table 1. I/O CONNECTOR DESCRIPTION

Pin Name	Pin Type	Description	Value
GND	①	Signal ground on the driver	0 V
VCC	②	Bias voltage for high current driver	4.5 V < Vcc < 5.5 V
LIN	③	Logic input for low-side gate driver	0 V < LIN< Vcc + 0.3 V
HIN	④	Logic input for high-side gate driver	0 V < HIN< Vcc + 0.3 V

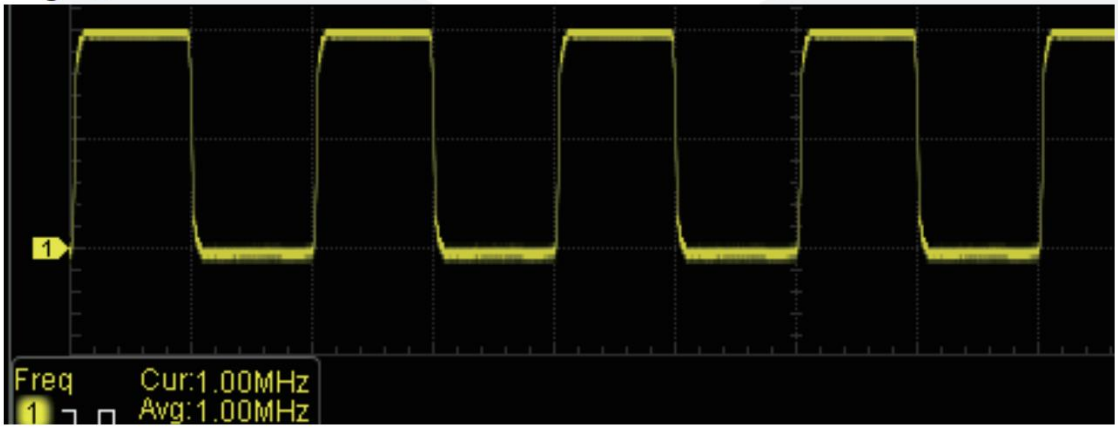
Vgs @200kHz



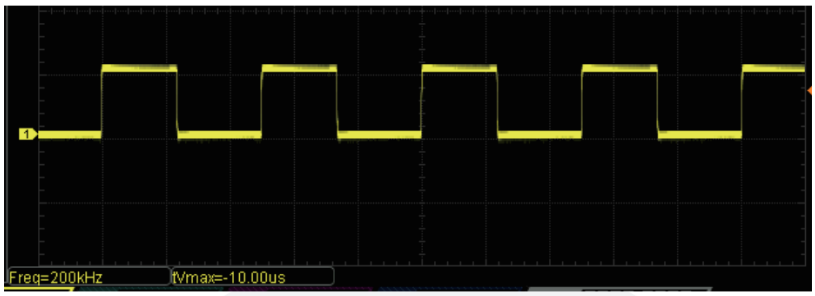
Vgs @1MHz VDD = 100V



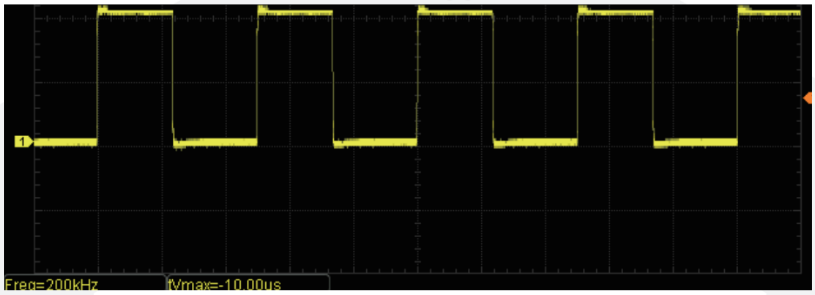
Vgs @1MHz VDD = 200V



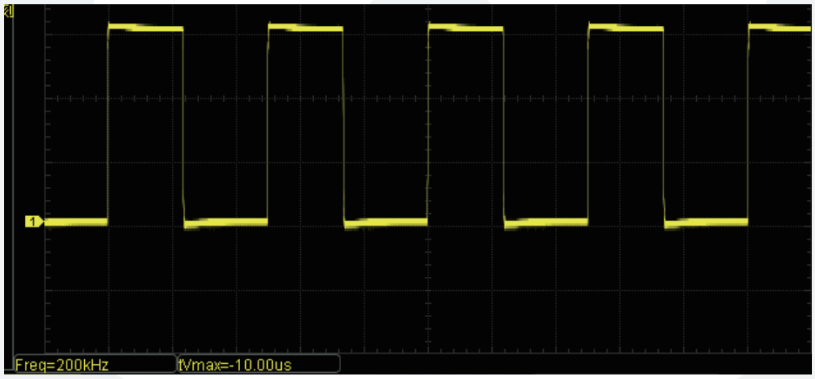
Vgs @200kHz, VDD = 100V



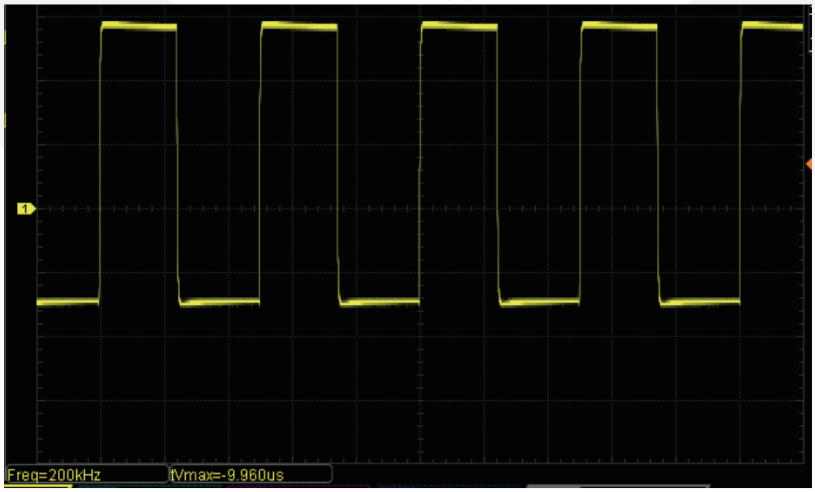
VDD = 200V



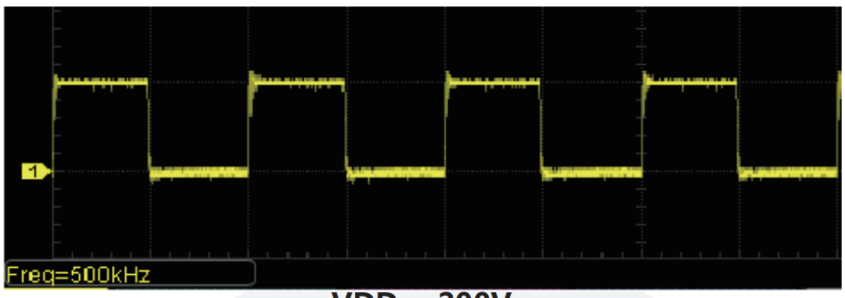
VDD = 300V



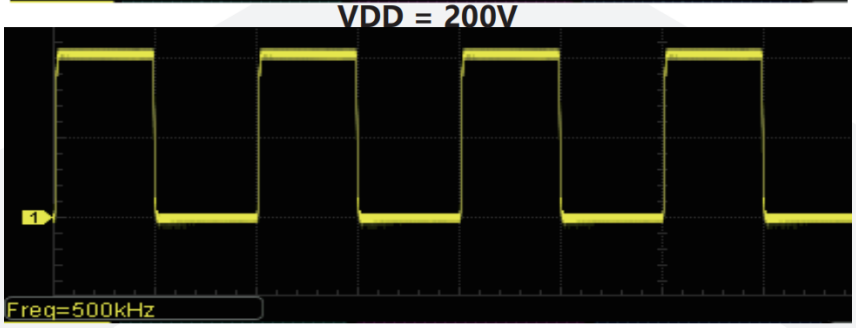
VDD = 400V



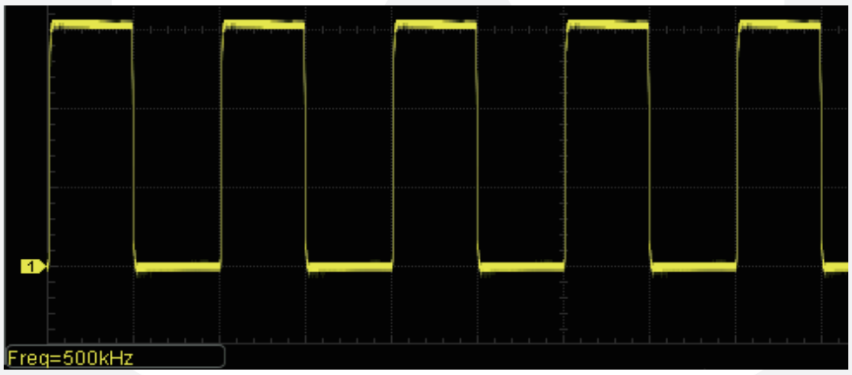
Vgs @500kHz, VDD = 100V



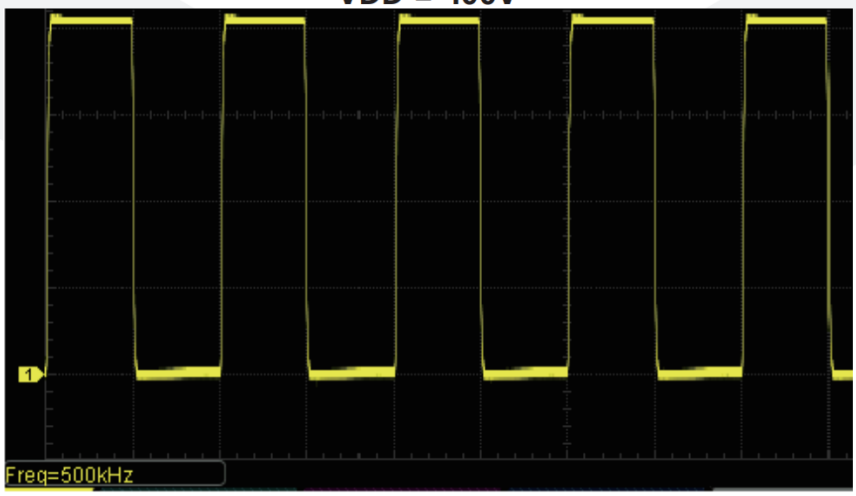
VDD = 200V



VDD = 300V



VDD = 400V



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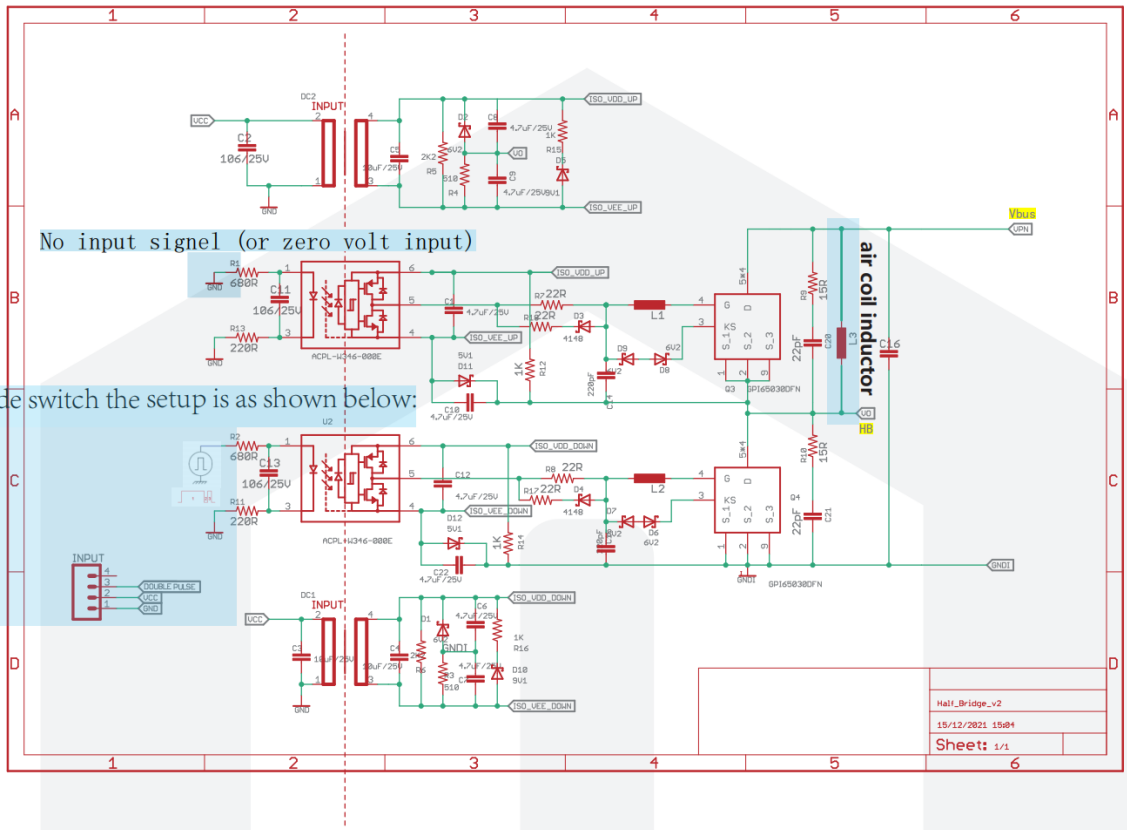
- **Double pulse test**

Jan. 2022

Double pulse test

The double pulse test is used to evaluate the switching characteristics of a power switch under hard switching but in a safe manner.



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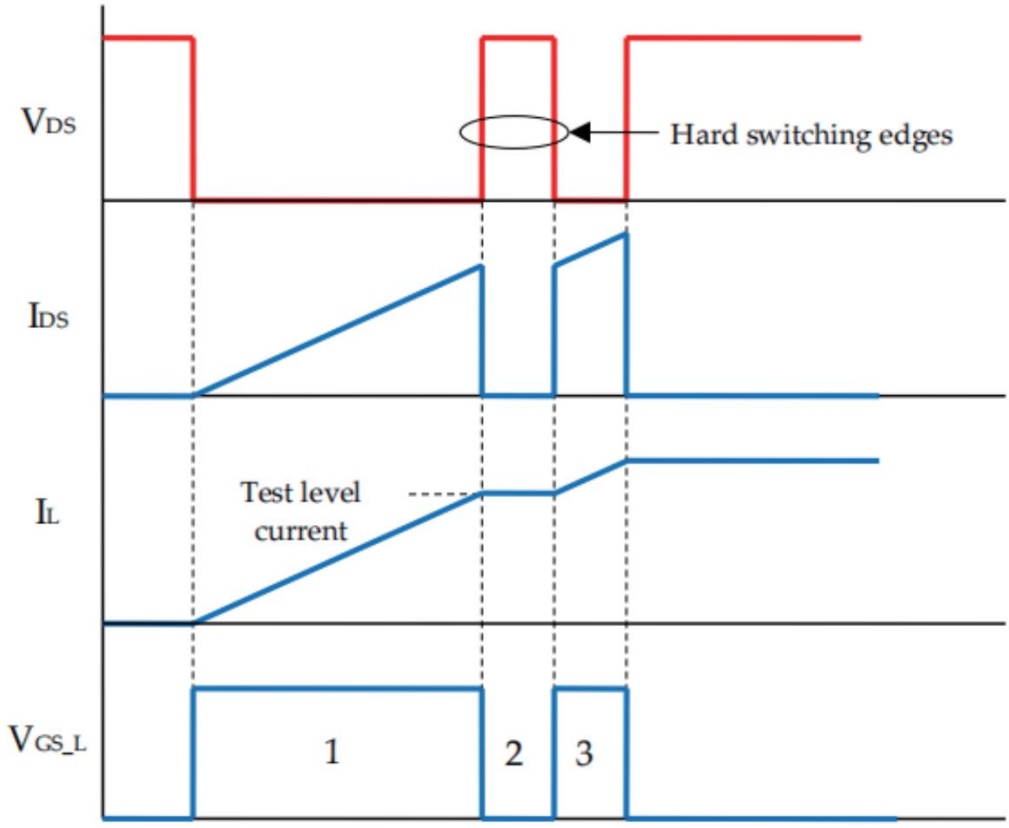
The low side switch is driven with two pulses as shown below. The high side switch can be held off or driven with the inverse of the low side gate switch (with adequate dead time).

Remarks:

1. Disable high side input signal

2. Lower side connected with double pulse signal

3. Connect the air coil inductor between VBUS and HB



Double Pulse Test Waveforms

An inductor is placed in parallel with the high side switch. The goal of this inductor is to establish the test level current in the low side switch at the end of the first on pulse (1). The magnitude of the test level current at the end of period 1 is given by:

$$I_L = \frac{V_{BUS}\, T_{ON\_1}}{L}$$

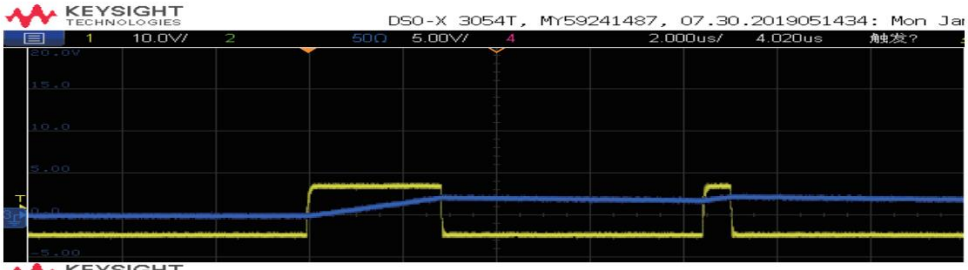
During period 2, the inductor current will naturally decay. The duration of period 2 should not be too long that inductor current deviates significantly from the desired test level.

During period 3, the inductor current will again rise. Period 3 should not be so long that the inductor current rises to an excessive level.

The falling edge of pulse 1 is used to examine the hard turn off characteristics of the switch. The rising edge of pulse 3 is used to examine the hard turn on characteristics of the switch. By only applying these two pulses, the switches are only on for a very short time and should not overheat.

DPT Result 100V 2A-27A

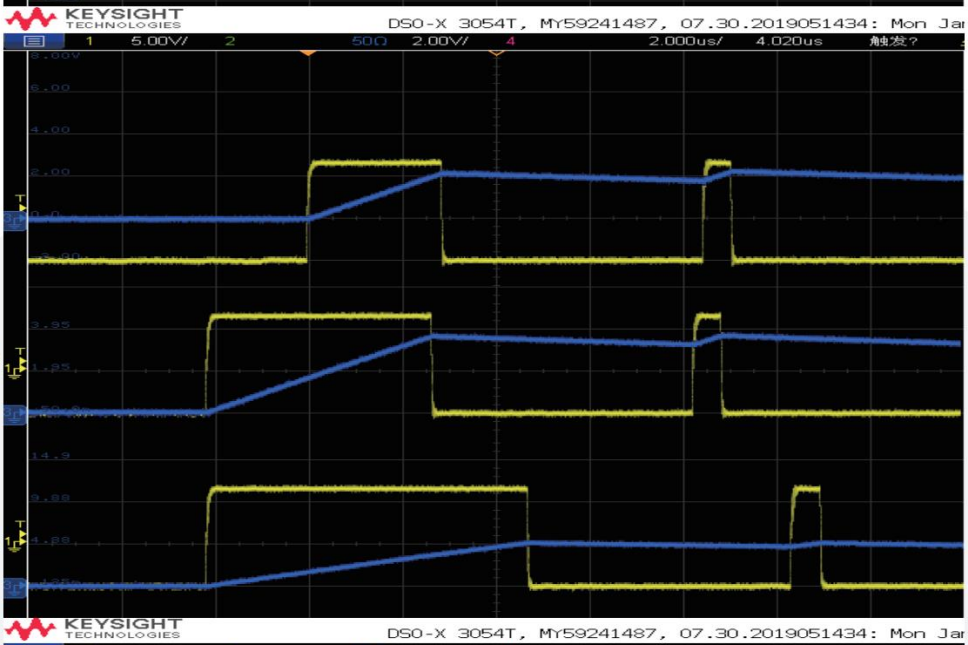
2A



6A

10A

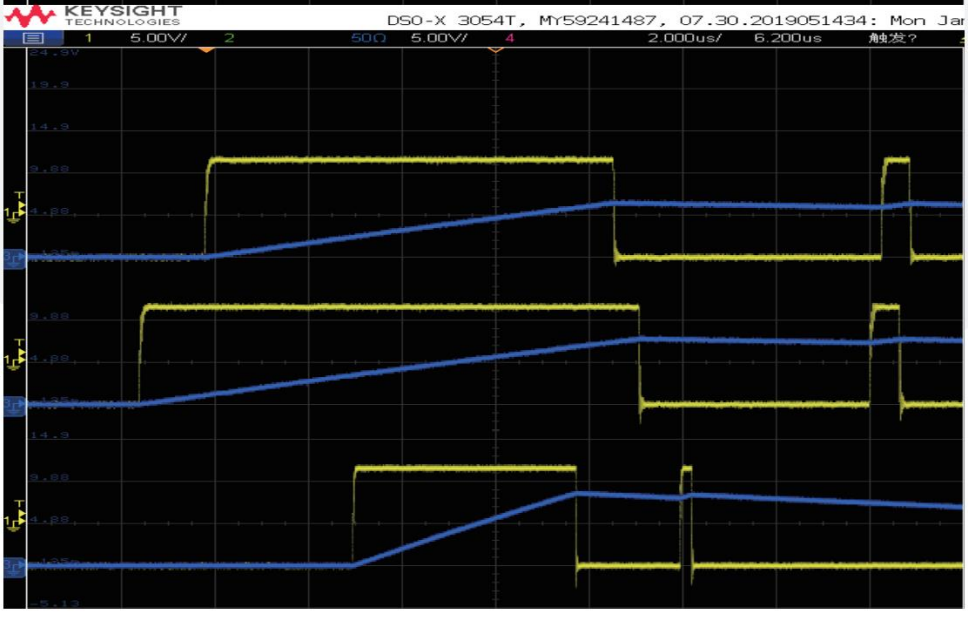
14A



18A

22A

27A



BOM

Comment	Designator	Footprint	Quantity
4.7uF/25V	C1, C12	1206:1	2
106/25V	C2, C11, C13	0805-CAP-MARKED:1	3
10uF/25V	C3, C4, C5	0805-CAP-MARKED:1	3
4.7uF/25V	C6, C7, C8, C9	0805-CAP-MARKED:1	4
4.7uF/25V	C10, C22	1206:1	2
220pF	C14, C15	0603-CAP-MARKED:1	2
	C16	C275-173X316@1	1
22pF	C20, C21	0805-CAP-MARKED:1	2
6V2	D1, D2	TIMWOO-DIODES_SMA-DIODE	2
4148	D3, D4	TIMWOO-DIODES_SOD-123	2
9V1	D5, D10	TIMWOO-DIODES_SMA-DIODE	2
6V2	D6, D7, D8, D9	TIMWOO-DIODES_SOD-123	4
5V1	D11, D12	TIMWOO-DIODES_SMA-DIODE	2
	DC1, DC2	DC-DC	2
	INPUT	04P	1
	L1, L2	L2012C	2
GPI65030DFN	Q3, Q4	DFN8X8_9PIN	2
680R	R1, R2	R0603	2
510	R3, R4	RESISTORS_1206:2	2
2K2	R5, R6	RESISTORS_1206:2	2
22R	R7, R8, R17, R18	R0603	4
15R	R9, R10	R0805	2
220R	R11, R13	R0603	2
1K	R12, R14	R0603	2
1K	R15, R16	RESISTORS_1206:2	2
ACPL-W346-000E	U1, U2	SOIC127P1150X360-6N	2

Thank you for using GaNPower!

Please send feedbacks., questions and comments to information@iganpower.com

07-01-2022 Ver 1.0