GaN Power HEMT Tutorial:
GaN Driving

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Gate Driving: Turn-on

Miller Plateau
Gate Driving: Turn-off

Miller Plateau

\( V_{GS,\text{final}} \)
\( V_{\text{plateau}} \)
\( V_{\text{th}} \)

\( I_{ds} \)
\( I_D \)

\( V_{ds} \)
\( V_D \)

\( V_D \)
\( V_{ds} \)

\( (V_{GS}=V_{GS,\text{final}}) \)
\( (V_{GS}=V_{\text{plateau}}) \)
Gate Driving: **Non-ideal case**

- **V_{gs}**
  - **V_{gs, final}**
  - **V_{plateau}**
  - **V_{th}

Caused by

- **I_d, overshoot**

Caused by **I_d, undershoot**

- **I_{ds}**
- **I_D**

**Q_{rr}** from the other transistor (for cascode) and charging current for **C_{OSS} (Q_{OSS})**

A portion of the **I_{ds}** has to charge **C_{OSS}**

- **V_{ds}**
- **V_D**

Drain leakage inductance induced

(V_{D} - L*di/dt)

- **V_{gs} - V_{th}**

Non-linearity of **C_{OSS}**

(V_{D} + L*di/dt)
Gate Driving: Switching Loss

\[ Q_{gs1} + Q_{gd} \]

\[ Q_{gs2} + Q_{gd} \]

Turn-on-Loss

Turn-off-Loss
Gate Driving: **Soft and Hard-switching Turning-on**

- **A1, A2: Hard Switching**
- **A1 Hard Turn-off**
- **B1, B2: Soft Switching**
- **B1 ZVS**
- **ZCS B2**

**Current Slope Determined by the Inductor**

**No Miller Plateau**

**ZVS Soft Switching**

**Hard Switch**

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Gate Driving: Turning-off with Strong Driver

- ZVS provides soft-switching at turning-on, but turning-off is still hard switching.
- A strong driver increases switching speed, reduces switching time and switching losses.
- For a strong driver turn-off, Miller plateau may not be observed. This is exactly what we have seen when switching GaN devices off.

Ref: Wei Zhang, Mastering the art and fundamentals of high voltage gate driver; TI High Volt Interactive
Gate Driving: Parasitic Inductance

- **Bonding-wire Inductance**: ~0.5 nH
- **Lead Inductance**: ~10 nH

**Diagram Details**:
- $L_{G,\text{EXT}}$, $L_{G,\text{IN}}$, $L_{S,\text{EXT}}$, $L_{S,\text{IN}}$
- $C_{GD}$, $C_{GS}$, $C_{DS}$
- $V_{\text{pulse}}$, $V_{D\text{D}}$
Gate Driving: Kelvin Source

Some device packaging types, such as DFN, have kelvin source pins, properly connecting the kelvin source to the drive loop will minimize the common source inductance (CSI)
Gate Driving: Parameters that affect switching loss

- Gate resistance $R_g$
- Gate to source capacitance $C_{GS}$
- Gate to drain capacitance $C_{GD}$
- Drain to source capacitance $C_{DS}$

[Diagram showing gate driving parameters]
Gate Driving: $R_g$

$R_g \uparrow$:

- $dv/dt \downarrow$
- $di/dt \downarrow$
- Reduces switching speed
- Increase switching loss
Gate Driving: $R_g$ (Experimental)

- $R_g$ limits the gate charging and discharging current and reduces $dv/dt$ and $di/dt$ slew rate.
- Larger $R_g$ will increase switching loss, especially for turn-off.
- A properly selected $R_g$ can mitigate the EMI issue that stems from high switching speed.

Gate Driving: $R_g$ Design Considerations

Trade off between **fast switching** and **ringing**

- Equivalent RLC circuit for voltage driven topology:
  - Small $R_g \downarrow$ ⇒ fast switching $\uparrow$ ⇒ large ringing $\uparrow$
  - Large $R_g \uparrow$ ⇒ slow switching $\downarrow$ ⇒ small ringing $\downarrow$

- Ringing causes Conducted Electromagnetic Interference (CEMI)

$$R_G \geq \sqrt{\frac{4(L_G + L_S)}{C_{GS}}}$$

http://www.electronicdesign.com/power/take-practical-path-toward-high-performance-power-conversion

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Gate Driving: $R_g$ Design Considerations

- To avoid ringing, with certain $L_G$, $L_S$ and $C_{GS}$, $R_G$ can be calculated as:

$$R_G \geq \sqrt{\frac{4(L_G + L_S)}{C_{GS}}}$$

For GPI65015DFN with $C_{GS} = 119$ pF

<table>
<thead>
<tr>
<th>$L_G + L_S$ (nH)</th>
<th>$R_G$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>5.8</td>
</tr>
<tr>
<td>2</td>
<td>8.2</td>
</tr>
<tr>
<td>3</td>
<td>10.0</td>
</tr>
<tr>
<td>4</td>
<td>11.6</td>
</tr>
</tbody>
</table>

http://www.electronicdesign.com/power/take-practical-path-toward-high-performance-power-conversion
Gate Driving: $C_{GS}$

$C_{GS} \uparrow$:

- $dv/dt$ -
- $di/dt \downarrow$
- $C_{GS}$ mostly affects the current rising and falling period

Charging $C_{GS} \rightarrow di/dt$
Gate Driving: $C_{GD}$

$C_{GD}$ $\uparrow$:

- $dv/dt$ $\downarrow$
- $di/dt$ $-$
- $C_{GD}$ mostly affects the drain rising and falling period during the Miller plateau

Charging $C_{GD}$ $\rightarrow$ $dv/dt$
Gate Driving: Adding External $C_{DS}$

- Adding external $C_{DS}$ capacitance does not reduce $dv/dt$ at turn-on.
- When the device turns on, at Miller plateau, drain voltage drops from $V_D$ to 0.
- $dv/dt$ is governed by the $C_{gd}$ and discharging current $I_{gd}$ from the gate driver.
- Paralleling external capacitance to $C_{ds}$ doesn’t impact $dv/dt$ at turn-on, but it will add extra channel current $I_{CDS}$ that increases switching loss for hard-switching.
Gate Driving: Adding External $C_{DS}$

- When the device turns off, at Miller plateau, drain voltage rises from $0$ to $V_D$.

- $I_{DS}$ from the drain is diverted into three parts: $I_{gd}$ for charging $C_{GD}$, $I_{CDS}$ for charging $C_{DS}$, and the rest goes through the channel ($I_{channel}$).

- $dv/dt$ at turning-off is governed by $C_{GD}$ and $C_{DS}$. Increasing $C_{DS}$ will reduce $dv/dt$, especially if $I_{channel}$ is relatively small.

- $I_{CDS}$ will divert the current in the channel and reduces switching loss at turn-off (but increases turning-on loss at the same time for hard switching).

- If paralleling $C_{DS}$ is required to improve EMI, the value should be large enough so that the $dv/dt$ rate at turn-off can be modulated.
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High dv/dt Effect

- High dv/dt charges parasitic capacitances. $C_{DS}$ is charged during this period, as well as the series connected $C_{GD}$ and $C_{GS}$

- If the $V_{GS}$ gets higher than $V_{th}$ due to $C_{GS}$ charging, the device unintentionally switches on, which will lower overall efficiency. This is called Miller turn-on

- A by-pass can divert the current that flows through Miller capacitance to avoid false turn-on

- Miller ratio ($Q_{GD}/Q_{GS1}$) can be used to determine how fragile the devices are due to Miller false turn-on. If the ratio smaller than 1, the device is guaranteed no false turn-on. However, many commercial devices cannot keep the ratio below 1

- Miller ratio also depends on applied $V_{ds}$, since $Q_{gd}$ is a function of $V_{ds}$. Higher $V_{ds}$ yields larger $Q_{gd}$ and thus more sensitive to dv/dt
GaN Device \(dv/dt\) issue: no pull-down path

With no pull-down current from external driver:

\[
V_{GS} = V_{DS} \frac{C_{GD}}{C_{GS} + C_{GD}}
\]

In order to maintain \(V_{GS} < V_{TH}\) so that GaN device won’t suffer from false turn-on, the maximum \(V_{DS}\) can be calculated as:

\[
V_{DS,max} \leq V_{TH} \frac{C_{GS} + C_{GD}}{C_{GD}}
\]

The calculated \(V_{DS,max}\) value can be quite small.

Texas Instruments: Estimating MOSFET Parameters from the Data Sheet
GaN device dv/dt Issue: The intrinsic dv/dt limit

If the external driver resistance is 0, which means G and S are shorted, this is to calculate the intrinsic dv/dt limit

\[ C_{GD} \frac{dV_{DS}}{dt} R_{G,I} \leq V_{TH} \]

\[ \Rightarrow \left. \frac{dV_{DS}}{dt} \right|_{\text{max}} \leq \frac{V_{TH}}{C_{GD} \cdot R_{G,I}} \]

For example: \( C_{GD} = C_{rss} = 4 \text{ pF (}@V_{DS} = 400\text{V)}; \ C_{GS} = C_{iss} - C_{rss} = 123 - 4 = 119 \text{ pF (}@V_{DS} = 400\text{V)}; \ R_{G,I} = 1.5\Omega \)

\[ \left. \frac{dV_{DS}}{dt} \right|_{\text{max}} \leq \frac{V_{TH}}{4 \text{pF} \times 1.5\Omega} = \frac{1.41\text{V}}{6\Omega} = 235\text{V/\text{ns}} \]
GaN device $dv/dt$ issue: A practical design

In a **practical design**, with external gate resistance $R_{GATE}$ and driver resistance $R_{LO}$

For example: $C_{GD} = C_{rss} = 4 \, \text{pF}; \, C_{GS} = C_{iss} - C_{rss} = 123 - 4 = 119 \, \text{pF}; \, R_{G,I} = 1.5 \, \Omega$; with gate driver from TI UCC27611: $R_{LO} = 0.35 \, \Omega$; and assume $R_{GATE} = 0.5 \, \Omega$ and @$V_{DS}=400\,\text{V}$

$$\Rightarrow \left| \frac{dV_{DS}}{dt} \right|_{\text{max}} \leq \frac{V_{TH}}{C_{GD} \cdot (R_{G,I}+R_{GATE} + R_{LO})} = \frac{1.41\,\text{V}}{4\,\text{pF} \cdot (1.5\,\Omega + 0.35\,\Omega + 0.5\,\Omega)} = 150\,\text{V/ns}$$

Low impedance turn-off drive-loop is critical for designs with GaN due to high $dv/dt$, especially for 650V devices
GaN device \( \frac{dv}{dt} \) issue: A more comprehensive approach

A more comprehensive analysis was done by a group of researchers at Virginia Tech for MOSFET before, and it can be applied to GaN as well.

Besides \( C_{gd} \), other parasitic components such as \( L_d \), \( L_s \), \( C_{gs} \) and \( C_{ds} \) all play a role in spurious turn-on by high drain \( \frac{dv}{dt} \).

This is another reason why we should have lower parasitic inductance.

\[
\left. \frac{dV_{DS}}{dt} \right|_{max} \leq \frac{V_{TH}}{C_{gd}R_{gs} + C_{gd}\left(\frac{1}{C_{gs}} - \frac{R_{gs}^2}{4L_g}\right)\sqrt{(L_d + L_s)(C_{gd} + C_{ds})}}
\]

Yuming Bai, Deva Pattanayak*, Alex Q. Huang, Analysis of \( dv/dt \) Induced Spurious Turn-on of MOSFET, Virginia Tech
GaN $dv/dt$ issues: High Side

- With high positive and negative $dv/dt$ slew rate of GaN, the common mode current can flow through the level-shifter or isolator of the high side switch.

- It can cause ground bounce within the level shifter and even change logic states.

- A smaller parasitic capacitance from the level-shifter or isolator is desirable, which will give a higher CMTI (common mode transient immunity).
GaN vs. SJ MOS in terms of $dv/dt$

GaN - Cascode  
State-of-Art Silicon

<table>
<thead>
<tr>
<th>Parameter</th>
<th>600V Si</th>
<th>600V GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>600V</td>
<td>600V</td>
</tr>
<tr>
<td>$R_{DS}$</td>
<td>0.14$\Omega$</td>
<td>0.15$\Omega$</td>
</tr>
<tr>
<td>$C_{OSS(Tr)}$</td>
<td>314pF$^2$</td>
<td>71pF$^2$</td>
</tr>
<tr>
<td>$Q_{rr}$</td>
<td>8200nC$^3$</td>
<td>42nC$^4$</td>
</tr>
<tr>
<td>$t_{rr}$</td>
<td>460ns$^3$</td>
<td>24ns$^4$</td>
</tr>
</tbody>
</table>

- GaN has much higher $dv/dt$ and $di/dt$ than SJ MOS, special designs are necessary and drivers with high CMTI (Common mode transient immunity) is necessary.

Wei Zhang, A Deep Dive of Isolated Gate Driver Robustness – $dv/dt$ (CMTI) and $di/dt$, TI, APEC 2018
Common Source Inductance (CSI) and \( \text{di/dt} \) issues

- The common source inductance (CSI) is shared by the power loop and the drive loop.
- Voltage across the CSI will be induced by the high current slew rate \( \text{di/dt} \) during switching period.
- During device turn-on, this voltage counteracts with the voltage on the gate and elongates the turn-on time.
- During device turn-off, this voltage increases the gate voltage, delays the turn-off time and causes ringing and false turn-on.
- This negative feedback brings longer voltage-current overlap and increases switching loss.
- A Kelvin pin is generally required to separate power and driving loop.

<table>
<thead>
<tr>
<th>Type</th>
<th>( L_G ) (nH)</th>
<th>( L_S ) (nH)</th>
<th>( L_D ) (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TO220</td>
<td>3.6</td>
<td>3.9</td>
<td>2.3</td>
</tr>
<tr>
<td>DFN</td>
<td>2.4</td>
<td>0.9</td>
<td>1.3</td>
</tr>
</tbody>
</table>
Ground Bounce

- If controller ground is tied to the power ground, the controller logic might be affected by the voltage pulses on the CSI (created by large high voltage slew rates across capacitors that generates large current pulses of short duration), which is called “ground bounce”

- Ground bounce can alter the normal device switching and lead to unwanted device behaviors

- One way to mitigate this issue is to tie the controller ground to the driver ground
DFN vs. TO220 GaN in Hard-Switching (CSI Issue)

- CSI affects di/dt, not dv/dt
- For turn-on, a lower di/dt can be observed for TO220 with CSI and no kelvin pin (due to Ig↓)
- Voltage transition is postponed due to increased current transition time
- Higher $E_{on}$ loss for TO220

- For turn-off, there is no voltage transition delay, since voltage rises before current falls
- di/dt rate is not much different, since most of the current transition we observed are for $C_{oss}$ charging
- However, a severe ringing occurred in TO220 that may indicate a false turn-on. $E_{off}$ loss is higher for TO220

Xiucheng Huang, Tao Liu, Bin Li, Fred C. Lee, and Qiang Li; Evaluation and Applications of 600V/650V Enhancement-Mode GaN Devices, 2015 WiPDA
Gate Driving: Bootstrap

- If a bi-polar gate voltage (negative for turning-off) is applied, $V_{sd}$ for GaN devices can be quite large (several Volt)

- Bootstrap capacitor can be over-charged to cause damage to upper GaN switch

$$V_{cap} = V_{DD} - V_{diode} + V_{sd}$$
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Gate Voltage Requirements

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_{ds}$ Ratings</th>
<th>Optimal $V_{gs}$</th>
<th>Max $V_{gs}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si-MOS</td>
<td>20~650V</td>
<td>-10~+15V</td>
<td>±20V</td>
</tr>
<tr>
<td>Si-IGBT</td>
<td>≥650V</td>
<td>-5~+20V</td>
<td>±20V</td>
</tr>
<tr>
<td>SiC-MOS</td>
<td>≥650V</td>
<td>-5~+6V</td>
<td>-10~+25V</td>
</tr>
<tr>
<td>GaN</td>
<td>≤1200V</td>
<td>-10~+7V</td>
<td>-10~+7V</td>
</tr>
</tbody>
</table>
# Commercial Discrete 650V E-Mode GaN Driver Examples

<table>
<thead>
<tr>
<th>GaN Drivers</th>
<th>Vendor</th>
<th>Configuration</th>
<th>Sink / Source</th>
<th>VDD Supply Voltage</th>
<th>Gate Drive Voltage</th>
<th>Pull-up / Pull-down Resistance</th>
<th>Propagation Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM5114</td>
<td>TI</td>
<td>Single-Sided</td>
<td>7.6A / 1.3A</td>
<td>4~12.6V</td>
<td>~VDD</td>
<td>2Ω / 0.23Ω</td>
<td>12ns</td>
</tr>
<tr>
<td>UCC27611</td>
<td>TI</td>
<td>Single-Sided</td>
<td>4A / 6A</td>
<td>4~18V</td>
<td>5V</td>
<td>1Ω / 0.35Ω</td>
<td>14ns</td>
</tr>
<tr>
<td>UCC27517</td>
<td>TI</td>
<td>Single-Sided</td>
<td>4A/4A</td>
<td>4.5~18V</td>
<td>~VDD</td>
<td>5Ω / 0.5Ω</td>
<td>13ns</td>
</tr>
<tr>
<td>MAX5048C</td>
<td>Maxim Integrated</td>
<td>Single-Sided</td>
<td>7A / 3A</td>
<td>4~14V</td>
<td>~VDD</td>
<td>0.84Ω / 0.3Ω</td>
<td>8ns</td>
</tr>
<tr>
<td>FAN3122</td>
<td>Fairchild / ON-Semi</td>
<td>Single-Sided</td>
<td>9.7A / 7.1A</td>
<td>4.5V to 18V</td>
<td>~VDD</td>
<td>NA</td>
<td>20ns</td>
</tr>
<tr>
<td>Si8271</td>
<td>Silicon Lab</td>
<td>Single-Sided</td>
<td>4A / 4A</td>
<td>4.2V to 30V</td>
<td>~VDD</td>
<td>2.7Ω / 1Ω</td>
<td>60ns (max)</td>
</tr>
<tr>
<td>Si8273</td>
<td>Silicon Lab</td>
<td>Half-bridge</td>
<td>4A / 4A</td>
<td>4.2V to 30V</td>
<td>~VDD</td>
<td>2.7Ω / 1Ω</td>
<td>60ns (max)</td>
</tr>
<tr>
<td>NCP51820</td>
<td>ON</td>
<td>Half-Bridge</td>
<td>2A/1A</td>
<td>9V to 17V</td>
<td>5.5V</td>
<td>N/A</td>
<td>25ns</td>
</tr>
</tbody>
</table>
Isolated Gate Driving

In order to meet IEC 61010 isolation requirement, three types of isolated gate driving are available:

- **Gate Isolation with Transformer**
- **Gate Isolation with Digital Isolator**
- **Isolated Gate Driver**

<table>
<thead>
<tr>
<th></th>
<th>Transformer Iso</th>
<th>Digital Isolator</th>
<th>Isolated driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prop. Delay</td>
<td>20 ns</td>
<td>100 ns</td>
<td>19 ns (Typical)</td>
</tr>
<tr>
<td>Bias Power</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>$C_{IO}$</td>
<td>$\geq 10$ pF</td>
<td>$&lt; 1$ pF</td>
<td>$&lt; 1$ pF</td>
</tr>
<tr>
<td>Parasitics</td>
<td>Large $L_{ik}$</td>
<td>Very Small</td>
<td>Very Small</td>
</tr>
<tr>
<td>Overshoot</td>
<td>Large</td>
<td>Small</td>
<td>Small</td>
</tr>
<tr>
<td>Size</td>
<td>Bulky</td>
<td>Small</td>
<td>Very Small</td>
</tr>
</tbody>
</table>

Source: Wei Zhang, Mastering the art and fundamentals of high voltage gate driver; TI High Volt Interactive
Half Bridge Gate Driver: Isolated and Non-Isolated

A typical non-isolated gate driver from TI

Isolated gate driver such as Si8273 provides:

- 200 kV/μs CMTI
- 2.5 kV RMS withstand voltage
- Input supply: 2.5–5.5 V
- Driver supply: 4.2–30 V (6V for E-mode GaN)
- Prop. Delay: 60 ns (max)

UCC27714 High-Speed, 600-VHigh-SideLow-SideGateDriver with 4-A Peak Output


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Digital Isolation Technology: Magnetic Isolator

Magnetic isolator is based on chip-scale transformers, compared to optocoupler, magnetic couplers use low-stress, thick-film polyimide insulation to achieve thousands of volts of isolation that can be monolithically integrated with standard silicon ICs and can be fabricated in single-channel, multi-channel, and bidirectional configurations.

- 4x improvement in data rate and timing specifications
- Integrates multiple isolation channels with other functions to reduce size and cost
- Operates at power levels up to 90% lower than optocouplers
- Minimizes external components needed to connect to other digital devices
- Increases reliability by eliminating LEDs used in optocouplers

Ref: Analog Devices: Standard Digital Isolators
Digital Isolation Technology: Capacitive Isolator

Capacitive isolation is made by adding capacitive isolation barrier on top of each die to connect in series, digital circuits are used for encoding and decoding various signals through the isolation barrier. A capacitive isolator’s inability to pass DC signals makes it inherently the right choice for isolation.

3. TI: Digital Isolators

Silicon Lab’s capacitive isolation solution

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# Isolation Technology: Comparison

<table>
<thead>
<tr>
<th></th>
<th>Isolation</th>
<th>$dv/dt$ immunity</th>
<th>Propagation delay</th>
<th>Integration level</th>
<th>Independent power supply needed at the secondary</th>
<th>Reliability (over time &amp; harsh environment)</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Optocouplers</strong></td>
<td>Few kV</td>
<td>$&gt;50kV/\mu s$</td>
<td>$&gt;400$ns</td>
<td>Medium</td>
<td>Yes</td>
<td>Aging issues</td>
<td>$</td>
</tr>
<tr>
<td><strong>Fiber optic</strong></td>
<td>Several 10’s kV</td>
<td>$&gt;100kV's/\mu s$</td>
<td>Negligible</td>
<td>Medium</td>
<td>Yes</td>
<td>Good reliability</td>
<td>$$$$</td>
</tr>
<tr>
<td><strong>Monolithic level shifter</strong></td>
<td>None</td>
<td>50kV/\mu s</td>
<td>-</td>
<td>Integrated on the IC</td>
<td>No</td>
<td>-</td>
<td>$</td>
</tr>
<tr>
<td><strong>Pulse transformer</strong></td>
<td>Several kV</td>
<td>$&gt;50kV/\mu s$</td>
<td>$&lt;100$ns</td>
<td>Bulky</td>
<td>No</td>
<td>Reliable</td>
<td>$</td>
</tr>
<tr>
<td><strong>Digital isolation</strong></td>
<td>Several kV</td>
<td>$&gt;100kV/\mu s$</td>
<td>~20 ns</td>
<td>Integrated on-chip or driver IC package</td>
<td>Yes</td>
<td>Very reliable</td>
<td>$$</td>
</tr>
</tbody>
</table>

### Diagram:

- **Fiber optic**: 
- **Optical**
- **Magnetic**
- **Capacitive**

**Source:**
Gate Drivers market evolution: coreless isolation and WBG specific solutions, Yole Development, APEC 2018

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Choosing GaN Gate Driver and $R_g$

- If possible, gate drivers with individual turn-on and turn-off pins are recommended.
- Use separate drive loops for turn-on and turn-off. Turn-off loop low impedance is recommended to avoid false turn-on and oscillations.
- Proper selection of $R_{g\text{-on}}$ vs. $R_{g\text{-off}}$ is critical. Normally the ratio of $R_{g\text{-on}}$ to $R_{g\text{-off}}$ can be chosen between 5 to 10.

*Source: GN001 Application Guide: Design with GaN Enhancement mode HEMT, GaN Systems*
Current-source and Voltage-source Gate Drivers

<table>
<thead>
<tr>
<th>Current-source gate driver</th>
<th>Voltage-source gate driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>➢ Current sources have a high resistive output by default</td>
<td>➢ Voltage sources shall be as low resistive as possible</td>
</tr>
<tr>
<td>➢ Any additional voltage drop in the gate drive loop has no influence on the gate current $I_g$ inside limits</td>
<td>➢ Any additional voltage drop in the gate drive loop has immediate influence on the gate current $I_g$</td>
</tr>
<tr>
<td>➢ Supposed to damp oscillations</td>
<td>➢ Prone to oscillations</td>
</tr>
</tbody>
</table>

Ref: Turn-on performance comparison of current-source vs. voltage-source gate drivers, Infineon, APEC 2018
Contents

- Session 1: GaN devices basics
- Session 2: GaN Gate Driving
  - Gate driving basics
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  - Gate drive related power loss calculations
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GaN Device Power Loss Analysis

- **Conduction Loss:**
  \[ P_{\text{Cond}} = I_D^2 \cdot R_{\text{ds(on)} \cdot D} \]  
  (D: Duty Cycle)

- **Switching Loss:**
  \[ P_{\text{Switching}} = \frac{1}{2} \cdot I_D \cdot V_D \cdot (t_{\text{on}} + t_{\text{off}}) \cdot f_{\text{sw}} \]

- **Gate Driving Loss:**
  \[ P_{\text{Driving}} = V_g \cdot Q_g \cdot f_{\text{sw}} \]

- **Power Loss from \( C_{\text{oss}} \):**
  \[ P_{\text{COSS}} = E_{\text{oss}} \cdot f_{\text{sw}} \]
GaN Gate Driving Loss

With same gate driver, soft-switching such as ZVS has a lower turn-on gate driving loss than hard-switching:

\[ P_{gate\_dr\_on} = E_{on\_soft} \cdot f_{sw} = V_{gs} \cdot Q_{gon\_soft} \cdot f_{sw} \]

\[ P_{gate\_dr\_on} = E_{on\_hard} \cdot f_{sw} = V_{gs} \cdot Q_{gon\_hard} \cdot f_{sw} \]
GaN vs. SJ MOS: $Q_{rr}$ and $Q_{OSS}$ Loss

SJ MOSFET with $Q_{rr}$ from body-diode and $Q_{OSS}$

GaN HEMT with $Q_{OSS}$ from other GaN


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GaN Device Power Loss Analysis: Hard-Switching

- With same $R_{dson}$ and same frequency, GaN power loss vs. Si:

\[
P_{\text{hard\_sw}} = P_{\text{cond}} + P_{\text{sw}} + P_{\text{coss}} + P_{\text{gate}} + P_{sd} + P_{rr}
\]

<table>
<thead>
<tr>
<th></th>
<th>SJ MOS</th>
<th>GaN</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{\text{cond}}$</td>
<td>same</td>
<td>same</td>
<td>Same $R_{dson}$</td>
</tr>
<tr>
<td>$P_{\text{sw}}$</td>
<td>higher</td>
<td>lower</td>
<td>Due to GaN has smaller $Q_{GS2}$ and $Q_{GD}$</td>
</tr>
<tr>
<td>$P_{\text{coss}}$</td>
<td>higher</td>
<td>lower</td>
<td>GaN has a lower $C_{oss}$</td>
</tr>
<tr>
<td>$P_{\text{gate}}$</td>
<td>higher</td>
<td>lower</td>
<td>GaN has lower gate drive voltage</td>
</tr>
<tr>
<td>$P_{sd}$</td>
<td>lower</td>
<td>higher</td>
<td>GaN has a higher $V_{sd}$</td>
</tr>
<tr>
<td>$P_{rr}$</td>
<td>higher</td>
<td>none</td>
<td>GaN has no $Q_{rr}$</td>
</tr>
<tr>
<td>$P_{\text{hard_sw}}$</td>
<td>higher</td>
<td>lower</td>
<td>GaN has a lower total hard switching power loss</td>
</tr>
</tbody>
</table>
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### GPI65030CO: Si driver basic parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ ($V_{DD}$ operating voltage)</td>
<td>$(T_J)$ range of $-40°C$ to $125°C$</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>UVLO</td>
<td>$V_{DD}$ under voltage lockout</td>
<td>$V_{DD}$ Rising</td>
<td>$T_J=25°C$</td>
<td>3.8</td>
</tr>
<tr>
<td>$V_{DD}$ undervoltage lockout hysteresis</td>
<td></td>
<td></td>
<td></td>
<td>0.2</td>
</tr>
<tr>
<td>$I_{DD}$ ($V_{DD}$ quiescent current)</td>
<td>$I_{D}=I_{NB}=0$</td>
<td>$T_J=25°C$</td>
<td>0.01</td>
<td>mA</td>
</tr>
<tr>
<td>N-CHANNEL OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{ON}$ ($R_{ON}$, Driver output resistance-pulling down)</td>
<td>$V_{DD}=5V$, $I_{N\text{-}OUT}=-100mA$</td>
<td>0.25</td>
<td>$\Omega$</td>
<td></td>
</tr>
<tr>
<td>$I_{PK\text{-}N}$ (peak sink current)</td>
<td>$C_L=10,000\ \text{pF}$</td>
<td>5</td>
<td>$A$</td>
<td></td>
</tr>
<tr>
<td>P-CHANNEL OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{OFF}$ ($R_{OFF}$, Driver output resistance-pulling up)</td>
<td>$V_{DD}=5V$, $I_{N\text{-}OUT}=50\ mA$</td>
<td>2.1</td>
<td>$\Omega$</td>
<td></td>
</tr>
<tr>
<td>$I_{PK\text{-}P}$ (peak source current)</td>
<td>$C_L=10,000\ \text{pF}$</td>
<td>1.3</td>
<td>$A$</td>
<td></td>
</tr>
</tbody>
</table>

### GPI65030CO: Si driver dynamic parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITION ($V_{DD}=5V$)</th>
<th>MIN</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{r}$ Rise time</td>
<td>$C_L=1nf$</td>
<td>5</td>
<td>$ns$</td>
<td></td>
</tr>
<tr>
<td>$t_{f}$ Fall time</td>
<td>$C_L=1nf$</td>
<td>3</td>
<td>$ns$</td>
<td></td>
</tr>
<tr>
<td>$t_{ON}$ turn-on propagation delay</td>
<td>$C_L=1nf$</td>
<td>$T_J=25°C$</td>
<td>17</td>
<td>$ns$</td>
</tr>
<tr>
<td>$t_{OFF}$ turn-off propagation delay</td>
<td>$C_L=1nf$</td>
<td>$T_J=25°C$</td>
<td>15.7</td>
<td>$ns$</td>
</tr>
<tr>
<td></td>
<td>$T_J=25°C$</td>
<td>$(T_J)$ range of $40°C$ to $125°C$</td>
<td>12.9</td>
<td>$ns$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(T_J)$ range of $-40°C$ to $125°C$</td>
<td>13.5</td>
<td>$ns$</td>
</tr>
</tbody>
</table>
Si Driver + GaN Co-package: D-Mode GaN

A smart gate driver IC for cascode D-GaN (By University of Toronto)

- Desired functions include
  - Tunable output resistance
  - Precise timing control
  - Current sensing for regulation and protections purposes

- Dynamic driving techniques
  - Change gate driving strength during switching

- Fully integrated controller circuits
  - Flexible digital control
  - Active driving ability under different load conditions

Jingshu Yu, Weijia Zhang, Andrew Shorten, Rophina Li and Wai Tung Ng, A Smart Gate Driver IC for GaN Power Transistors; ISPSD 2018
Si Driver + GaN Co-package: D-Mode GaN

On-chip Digital Controller

Segmented Gate Driver

Programmable sense-FET

Smart Gate Driver IC

10X D-Mode GaN by GaNPower

Jingshu Yu, Weijia Zhang, Andrew Shorten, Rophina Li and Wai Tung Ng, A Smart Gate Driver IC for GaN Power Transistors; ISPSD 2018

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Si Driver + GaN Co-package: E-GaN and SenseFET

A novel SenseFET by GaNPower helps researchers from University of Toronto won the prestigious 2019 IEEE ISPSD Charitat Young Researcher Award.

Source: W.J. Zhang, Y.H. Leng, J.S. Yu, Y.S. Lu, C.Y. Cheng and W.T. Ng, A Gate Driver IC for Enhancement Mode GaN Power Transistors with Precise Dead-time Correction, ISPSD 2019
Si Driver + GaN Co-package: E-GaN and SenseFET

- The SenseFET from GaNPower is rated at 100V/20mΩ with two extra leads for the sensing gate and sensing source.
- The current of the sensing source is designed to have a small match ratio while providing accurate sensing. However, the novelty is to use the SenseFET in a voltage clamping circuit to detect reverse conduction of the e-mode GaN low side output device while protecting the detection circuit from the high voltage swing at the switching node.
- The duration of this reverse conduction is then corrected by adjusting the dead-time in the following switching cycle to ensure optimum power conversion efficiency.
- The GaN SenseFET is conveniently packaged in an 8×8 8-lead DFN package.

Source: W.J. Zhang, Y.H. Leng, J.S. Yu, Y.S. Lu, C.Y. Cheng and W.T. Ng, A Gate Driver IC for Enhancement Mode GaN Power Transistors with Precise Dead-time Correction, ISPSD 2019

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Direct-drive looks like a cascode method, in which a low voltage MOS is in series with high voltage D-mode GaN. The difference is that TI integrates the driver IC to drive the GaN directly, while the low voltage MOS is used to make the package normally-off.

The voltage slew rate can exceed 100V/ns

Source: LMG341xR070 600-V 70-mΩ GaN with Integrated Driver and Protection. TI datasheet
GaN IC, is it the future?

- Currently, mainstream GaN technology is using 6-inch wafer with 0.5um feature size

- This roughly equals to the silicon lateral BCD technology used 20 years ago

- GaN IC doesn’t have P-type HEMT, due to ion-implantation of p-type materials such as Mg and subsequent thermal anneal very difficult to handle

- Instead, GaN IC is either using Direct-Coupled FET Logic (DCFL) with both E-mode and D-mode devices, or just use D-mode devices in the IC design

- Resistors, capacitors are available in GaN IC, much like 20 years ago in silicon BCD technology

Panasonic GaN IC

- GaN-based Semiconductor Devices for Future Power Switching Systems; Hidetoshi Ishida, Ryo Kajitani, Yusuke Kinoshita, Hidekazu Umeda, Shinji Ujita, Masahiro Ogawa, Kenichiro Tanaka, Tatsuo Morita, Satoshi Tamura, Masahiro Ishida and Tetsuzo Ueda; IEDM 2016
- Navitas APEC 2019 Industry paper
GaN IC, is it the future?

- Both active devices, such as high voltage and low voltage D-mode and E-mode HEMT are available

- Passive components, such as GaN-FET-based rectifiers, MIM capacitors and 2DEG resistors are available for analog functions

Source: Kevin J. Chen, Oliver Häberlen, Alex Lidow, Chun lin Tsai, Tetsuzo Ueda, Yasuhiro Uemoto and Yifeng Wu, GaN-on-Si Power Technology: Devices and Applications IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 3, MARCH 2017
GaN IC, is it the future?

- One of the first published monolithically integrated GaN IC design with two generations using directly-coupled FET Logic that combines both D-mode and E-mode transistors

GaN IC, is it the future?

Numerous design has been reported for GaN IC, including simple logic functions such as NAND, NOR and comparators.

GaN integrated ESD protection circuit (<2% area) integrated to the gate of the power device on the GaN power device platform. Human body model ESD voltage on the gate can exceed 5 kV from −45 °C to 150 °C.

An over-voltage-protection (OVP) function offered by GaNPower provides gate voltage protection by clamping gate voltage below required maximum gate voltage of GaN when the driver output exceed the maximum.

Source: Kevin J. Chen, Oliver Häberlen, Alex Lidow, Chun lin Tsai, Tetsuzo Ueda, Yasuhiro Uemoto and Yifeng Wu, GaN-on-Si Power Technology:, Devices and Applications IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 3, MARCH 2017

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GaN IC, is it the future?

GaN integrated pre-gate driver (<5% area) integrated with a 120-mm E-mode GaN power device. Integration of devices shortens parasitic paths and thus achieves low ringing, short rise (8.5 ns) and fall (2.5 ns) time, and higher switching speed.

Need more detailed analysis from the application side to fully compare the benefits and drawbacks of using either monolithically integrated GaN solution or Si driver + GaN solution.

Source: Kevin J. Chen, Oliver Häberlen, Alex Lidow, Chun lin Tsai, Tetsuzo Ueda, Yasuhiro Uemoto and Yifeng Wu, GaN-on-Si Power Technology:, Devices and Applications IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 3, MARCH 2017
GaN IC, is it the future?

IMEC is offering GaN IC for MPW (multi-project-wafer) based on their GaN-on-SOI epitaxy. They have also demonstrated first high-side/low-side GaN-IC on chip with perfect isolation.

Perfect isolation between High Side and Low Side transistors in a GaN-based half-bridge on chip.

Source: https://www.imec-int.com/en/200mm-GaN-on-Si-technology

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GaN IC, is it the future?

- **Monolithic solution**
  - Power devices integrated with drivers and other analog IC functions

- **System-in-package solution**
  - Power devices and driver IC chips in the same package

(From Yole Development with modifications). Gate Drivers market evolution: coreless isolation and WBG specific solutions.

Yole Development, APEC 2018
GaN IC, is it the future?

While monolithic integration provides ultimate performance and eliminates on-board parasitics, silicon IC + GaN co-package can still provide more comprehensive functionalities -- at least for now.
GaNPower Future Integrated Modules

We provide advanced solutions using GaN
THANKS FOR WATCHING!

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