GaN Power HEMT Tutorial:
GaN Basics

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GaNPower International Inc.

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Contents

- Session 1: GaN devices basics
  - GaN, An Introduction
  - GaN Design, Fabrication and Testing
  - GaN Compact Modeling and Reliability
- Session 2: Gate Driving
- Session 3: GaN Applications
### Power Devices: History of Evolutions

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Devices</td>
<td>Power Diode Germanium</td>
<td>Thyristor Silicon</td>
<td>Power Bipolar Silicon</td>
<td>Power MOSFET Silicon</td>
<td>IGBT Silicon</td>
<td>Schottky diode Silicon Carbide</td>
<td>Power HEMT GaN</td>
</tr>
</tbody>
</table>

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It’s time to move on…

The diagram illustrates the evolution of power devices over time, comparing GaN and Si devices. The X-axis represents the year, ranging from 1978 to 2009. The Y-axis shows the Figure of Merit (FOM) for different types of devices: Bipolar, VFET, HEXFET, and TrenchFET. The comparison between GaN and Si devices is shown with bar charts for drive power, conduction loss, and switching loss. The GaN devices are highlighted with green bars, indicating lower power consumption compared to Si devices.

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# Material Properties Comparison

<table>
<thead>
<tr>
<th>Material Property</th>
<th>Silicon</th>
<th>SiC-4H</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band-gap (eV)</td>
<td>1.1</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>Critical Field (1E+6 V/cm)</td>
<td>0.3</td>
<td>3</td>
<td>3.5</td>
</tr>
<tr>
<td>Electron Mobility (cm²/V-Sec.)</td>
<td>1450</td>
<td>900</td>
<td>2000</td>
</tr>
<tr>
<td>Electron Saturation Velocity (1E+6 cm/Sec.)</td>
<td>10</td>
<td>22</td>
<td>25</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm²K)</td>
<td>1.5</td>
<td>3.8</td>
<td>1.3</td>
</tr>
<tr>
<td>Baliga Figure of Merit (FOM) = $\varepsilon_s \mu E_c^3$</td>
<td>1</td>
<td>675</td>
<td>3000</td>
</tr>
</tbody>
</table>
WBG Power Devices: Applications

GaN HEMT

Encroaching

SiC MOSFET

Silicon Super Junction MOSFET

Encroaching

Silicon IGBT

Source: Yole Development: How power electronics will reshape to meet 21st century challenges? ISPSD 2015
## Substrate Materials for GaN HEMT

<table>
<thead>
<tr>
<th>Attributes</th>
<th>Si sub.</th>
<th>SiC sub.</th>
<th>Sapphire</th>
<th>GaN sub</th>
</tr>
</thead>
<tbody>
<tr>
<td>Defect density (cm(^{-2}))</td>
<td>1E+9</td>
<td>5E+8</td>
<td>3E+8</td>
<td>1E+3 to 1E+5</td>
</tr>
<tr>
<td>Lattice mismatch (%)</td>
<td>17</td>
<td>3.5</td>
<td>-16</td>
<td>0</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm-k at 25 °C)</td>
<td>1.5</td>
<td>4.9</td>
<td>0.25</td>
<td>1.3</td>
</tr>
<tr>
<td>Coefficients of thermal expansions (%)</td>
<td>54</td>
<td>25</td>
<td>34</td>
<td>0</td>
</tr>
<tr>
<td>Off-state leakage</td>
<td>high</td>
<td>high</td>
<td>low</td>
<td>low</td>
</tr>
<tr>
<td>Reliability and yield</td>
<td>low</td>
<td>low</td>
<td>low</td>
<td>high</td>
</tr>
<tr>
<td>Lateral or Vertical device</td>
<td>lateral</td>
<td>lateral</td>
<td>lateral</td>
<td>lateral or vertical</td>
</tr>
<tr>
<td>Integration possibility</td>
<td>Very high</td>
<td>Moderate</td>
<td>Moderate</td>
<td>-</td>
</tr>
<tr>
<td>Substrate size (mm)</td>
<td>300</td>
<td>150</td>
<td>100</td>
<td>50</td>
</tr>
<tr>
<td>Substrate cost (relative)</td>
<td>Low</td>
<td>high</td>
<td>Low</td>
<td>Very high</td>
</tr>
</tbody>
</table>
Simplified E-GaN vs. LDMOS Device Structures
Simplified E-Mode vs. D-Mode GaN HEMT

E-Mode GaN HEMT

D-Mode GaN HEMT

Silicon Substrate

GaN Layer

2DEG Channel

AlGaN / GaN Buffer Layer

AlN Nucleation Layer

P-GaN

Al$_x$Ga$_{1-x}$N
Cascode GaN HEMT

**Good:**
- GaN is normally on by nature: easy to fabricate
- Si like gate control with higher $V_{th}$
- Reverse conduction with LV MOS body-diode

**Bad:**
- Comparatively lower performance
- Controlling silicon rather than GaN gate
- May need extra TVS device to protect MOS
- Difficult to match $C_{oss}$ of GaN and MOS
- Still has $Q_{fr}$

<table>
<thead>
<tr>
<th>Part ID</th>
<th>GaNPower GaN HEMT</th>
<th>Super Junction MOS</th>
<th>SiC</th>
<th>Cascode GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPI65015TO</td>
<td>xxxxxxxxx</td>
<td>xxxxxxxxx</td>
<td>xxxxxxxxx</td>
<td></td>
</tr>
<tr>
<td>Rated Voltage</td>
<td>650V</td>
<td>700V</td>
<td>650V</td>
<td>600V</td>
</tr>
<tr>
<td>$R_{on}$</td>
<td>92mΩ</td>
<td>125mΩ</td>
<td>100mΩ</td>
<td>150mΩ</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>3.3nC</td>
<td>35nC</td>
<td>51nC</td>
<td>6nC</td>
</tr>
<tr>
<td>$R_{on}*Q_g$</td>
<td>304</td>
<td>4375</td>
<td>5100</td>
<td>900</td>
</tr>
</tbody>
</table>
Cascode GaN HEMT

- Cascode can make package more complicated with 3 components and ceramic substrate
- Can be more expensive than pure E-mode
- Also, cascode is not feasible for low voltage (<200V) GaN, due to the $R_{dson}$ portion from MOS is too high:
  - for 600V device, $R_{dson}$ from MOS contribute less than 5%;
  - for 100V device, MOS can contribute more than 30% of the $R_{dson}$, which is impractical

2. Alex Lidow Johan Strydom Michael de Rooij David Reusch, GaN TRANSISTORS FOR EFFICIENT POWER CONVERSION, Wiley
Commercial E-Mode GaN HEMT with “p-GaN”

GIT: Gate with Ohmic Contact and Current Control

Gate with Schottky Contact and Current Control

1, Kevin J. Chen, Understanding the Dynamic Behavior in GaN-on-Si Power Devices and IC’s, Integrated Power Conversion and Power Management, 2018
2, Greco, G., Iucolano, F., & Roccaforte, F. Review of technology for normally-off HEMTs with p-GaN gate. Materials Science in Semiconductor Processing
Why no Avalanche Breakdown in GaN?

- GaN has a very high critical electric field (10 times that of Si, on par with SiO₂ or SiN already)
- Lateral device structure causes electric field crowding, particularly in overlying insulators
- GaN HEMT is more like a ceramic capacitor breakdown in the overlying insulators, where peak electric field took place
- If breakdown ever occurs, the device suffers permanent damage
- Design margin (>30%) for GaN is usually much higher than that of Si (which only has 10%)

Michael A Briere, “Understanding The Breakdown Characteristics Of Lateral GaN-Based HEMTs”
Why no P-type GaN HEMT Like PMOS?

- Si has both NMOS and PMOS, for NMOS, current is carried by electrons while in PMOS, current is carried by the holes

- However, for GaN HEMT, there is no P-type GaN HEMT yet

- First, ion implantation and subsequent annealing of magnesium in GaN is very difficult to achieve

- Second, hole mobility in GaN is very low (30 cm²/Vs for holes vs. 2000 cm²/Vs for electrons)

- GaN monolithic ICs are realized either by using complementary E-mode and D-mode GaN, or using E-mode GaN only
Why E-mode GaN $V_{g\text{-max}}$ is Limited to 7V

- Unlike a silicon MOS, the P-GaN / AlGaN / GaN can be viewed as a PIN diode structure with a depletion region.

- With in-situ doped p-type dopant (Magnesium) for p-GaN layer, the depletion region extends over the thickness of the GaN 2DEG channel for $V_g=0$V, thus interrupts the channel below the gate region.

- When a positive gate bias is applied, the 2DEG channel is re-established, yielding to on-state conditions.

- Gate leakage current increases with increasing gate voltage. Voltage beyond 7V will result in higher gate leakage current.

- For the P-GaN / AlGaN / GaN gate stack, a TDDB (Time Dependent Dielectric Breakdown) needs to be analyzed for proper max gate voltage with long term reliability concerns.

- It has been determined that maximum rating of 6~7V for p-GaN HEMT is most appropriate.
At large negative gate bias, electrons from the gate or substrate may leak to the trap states close to the 2DEG channel, creating a “virtual gate” and modulate the depletion region.
Current Collapse: TCAD Transient Simulation

- Stress
- Drain Voltage
- Gate Voltage
- Drain Current
- Voltage
- Before Stress
- After Stress

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GaN Power Device Supply Chain

Basic Semiconductor Materials

Substrate Epi-wafer Fabrications

GaNPower 6 inch GaN Wafer (real photo)

Packaging Testing

Final Power Supply Products

PCB Assembly UL, CE, CCC Certification

Packaged GaN Devices

GaN Power Device Supply Chain

GaNPower 6 inch GaN Wafer (real photo)
How GaN Power Devices Are Fabricated?

1. Device Design and Layout
2. Device Fabrication
3. Circuit Probing (Wafer level testing)
4. Packaging (Wire-bond)
4. Packaging (Bumping)
4. New Lead frame Design
5. Final Testing (Packaging Level)

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GaN Design Stage (TCAD Simulation)

P-GaN HEMT Device Structure

*Simulated using Ohmic Gate Contact*

(*) Simulated using Ohmic Gate Contact

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GaN Design Stage (TCAD Simulation)

Silicon Substrate

ΔIn

AlGaN Buffer Layer

AlGaN Buffer Layer

AlN Seed Layer

2DEG Electron conc. @ Equilibrium (0V on all Terminals)

2DEG Electron conc. @ $V_d=200V \ V_g=V_s=0$

2DEG Electron conc. @ $V_d=400V \ V_g=V_s=0$

Depletion Region Propagates

Simulated Using Crosslight NovaTCAD
GaN Design Stage (TCAD Simulation)

Potential Plot @
\[ V_d = 100V \quad V_g = V_s = 0V \]

Potential Plot @
\[ V_d = 700V \quad V_g = V_s = 0V \]

E-Field Plot @
\[ V_d = 100V \quad V_g = V_s = 0V \]

E-Field Plot @
\[ V_d = 700V \quad V_g = V_s = 0V \]

Insulator Region (SiN)

Simulated Using Crosslight NovaTCAD
GaN Design Stage (TCAD Simulation)

- In addition to stress caused by material lattice mismatch, the intrinsic stress from SiN layer can be defined in the process simulation. The stress profile can be used by the device simulator to calculate the piezoelectric polarization.

- Stress engineering may help to achieve enhancement mode?

Simulated Using Crosslight NovaTCAD
Fabrication Process Flow for GaN Epi-layer

The GaN Epi wafer is fabricated from either Si, SiC or Sapphire substrate. Each layer is deposited using MOCVD (Metal Organic Chemical Vapor Deposition) for low cost and high throughput.
A GaN-on-Sapphire HEMT Fabrication Example

1st Gen  First Generation

First Generation GaN HEMT: with breakdown voltage $BV = 480V$, $R_{on,sp} = 12m\Omega\cdot cm^2$

2nd Gen  Second Generation

Second Generation GaN HEMT (Standard Design): with breakdown voltage $BV = 700V$, $R_{on,sp} = 4m\Omega\cdot cm^2$

3rd Gen  Third Generation

Third Generation GaN HEMT (Novel Crystal Lattice Design): $BV = 850V$, $R_{on,sp} = 3m\Omega\cdot cm^2$
# Fabrication Steps (D-mode HEMT)

Simplified GaN-on-Sapphire HEMT Process Flow (GaN-on-silicon is similar):

<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Wafer Cleaning</td>
</tr>
<tr>
<td>2</td>
<td>Mask #1: Mesa Etching</td>
</tr>
<tr>
<td>3</td>
<td>RIE Mesa Etching</td>
</tr>
<tr>
<td>4</td>
<td>Mask #2: S/D Contacts</td>
</tr>
<tr>
<td>5</td>
<td>Ohmic Contact Deposition</td>
</tr>
<tr>
<td>6</td>
<td>Mask #3: Gate Lithography</td>
</tr>
<tr>
<td>7</td>
<td>Schottky Gate Deposition</td>
</tr>
<tr>
<td>8</td>
<td>Growth of Passivation Layer</td>
</tr>
<tr>
<td>9</td>
<td>Mask #4: Contact Hole Opening</td>
</tr>
<tr>
<td>10</td>
<td>Mask #5: Field plate and metallization</td>
</tr>
</tbody>
</table>

![Fabrication Steps Diagram](image)
A GaN-on-Sapphire HEMT Process Flow Example

1. Mask 01 – Mesa etch
   - Define a device area
   - Create isolation between devices

2. Mask 02 – S/D
   - Source and drain contact to AlGaN
   - The metal must be deposited after a completely clean process to eliminate layers between AlGaN and Metal

3. Deposit S/D metal
   - Deposit ohmic contacts on top of AlGaN as source and drain

4. Lift-off and Anneal
   - To improve contact quality
   - Bad annealing may dramatically degrade the device performance

5. Mask 03 – Gate
   - Define gate region
   - The alignment in this step is the most critical as it affects many parameters (L_{gd}, Gate on Mesa, design of field plate)

6. Gate Metal Deposition
   - Pre-clean is important for the Schottky barrier

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A GaN-on-Sapphire HEMT Process Flow Example

⑦ Gate metal Lift-off

⑧ SiN deposition (passivation)
- The first layer of SiN layer is for passivation
- It is important for decreasing the traps at the AlGaN surface
- Many device performances, including leakage current, threshold voltage, breakdown voltage, are related to the quality of this passivation
- This layer is also used for the field plates

⑨ Mask 04: S/D contact
- The source fingers are opened for field plates
- The S/D/G pads are opened
- All other area should be covered by SiN

⑩ Mask 05 – Field Plate

⑪ Field Plate Lift-off

⑫ Second SiN deposition
- covers the whole area
Circuit Probing (CP)

Circuit Probing can sort out bad dies from good dies by combining multiple test items, both room temperature and high temperature tests can be applied.

Test items example:

- $I_{dss}$: Drain leakage current
- $I_{gss}$: Gate leakage current
- $V_{th}$: Threshold voltage
- $R_{dson}$: On-state resistance
- $g_m$: Transconductance

Pass / Fail depends on specified range, bad dies are inked to avoid being picked up for further packaging.

https://www.mjc.co.jp/en/technology/
http://www.jemam.com/probe_card.htm
https://www.formfactor.com/
Circuit Probing (CP)

Failed sites are marked with ink and will not be picked for packaging afterwards.

In this example, we have:

- Total dies: 229
- Bad dies: 32
- Yield: 86%

Sometimes the CP specs are too tight, resulting in lower yield. But a too loose spec can lead to increased device early failures.
Simplified Packaging Steps

1. **Circuit Probe**
   - Tester head
   - Interface
   - Stage

2. **Probing Card**

3. **Wafer IQC**

4. **Taping**

5. **Wafer BG**

6. **De-Taping**

7. **Dicing**

8. **Low-k Grooving (option)**

9. **Mounting**

10. **Laser Marking**

11. **BSC Laminating (option)**

12. **BSM Evaporation (option)**

13. **AOI**

14. **Wire Bond**
   - Silicon Die
   - Wedge Bond
   - Aluminium Wire
   - Source Connection
   - Gate Connection
   - Copper Tab (Drain Connection)

15. **Tape & Reel**

16. **Visual Inspection**
   - Automatic microscope

17. **Label**

18. **Shielding**

19. **Packaging**
   - Reel
Final Test (FT)

Final test can identify problems with assembled devices, and it is the last test before shipment.

Test items example:

- $I_{dss}$: Drain leakage current
- $V_{th}$: Threshold voltage
- $R_{dson}$: on-state resistance
- $BV$: Breakdown voltage

Pass / Fail depends on specified range.

http://www.accotest.com/index.asp

Power device FT tester
GaN Packaging Types

DFN 8x8
DFN 6x8
LGA
TO 252
TO 220
GaN Device Parameter Testing

- **Static (DC) parameters testing**
  - $R_{dson}$, $V_{th}$, $BV$, $I_{dss}$, $I_{gss}$, $V_{sd}$, $R_g$, etc...

- **Dynamic parameters testing**
  - $C_{iss}$, $C_{rss}$, $C_{oss}$, $Q_g$, $Q_{gs}$, $Q_{gd}$, $Q_{rr}$, etc...

- **Double pulse testing** (for dynamic parameters)
  - $T_r$, $T_f$, $T_{dr}$, $dv/dt$, etc...

- **Thermal testing**
  - $R_{thjc}$, $R_{thja}$, etc...

- **SOA testing**
Parameter Testing: DC Parameters

- **Static (DC) parameters testing for GaN HEMTs**

  - $R_{\text{ds(on)}}$ is tested by applying a 6V gate bias, Kelvin connection should be applied if an impedance analyzer or a power device analyzer/curve tracer such as Keysight 1505A is used. Both room and high temperature $R_{\text{ds(on)}}$ can be recorded at certain drain current level (e.g. $I_d=5\,\text{A}$ for 100 mΩ device)

  - $V_{\text{th}}$ is tested by shorting drain and gate terminals and apply a voltage to the drain with respect to the source. The voltage is recorded at certain drain current level (e.g. 3.5 mA for 100 mΩ)
Parameter Testing: DC Parameters

- Static (DC) parameters testing for GaN HEMTs

- BV (breakdown voltage test) for GaN HEMT is very different from MOSFET. For $I_d - V_d$ breakdown curves are rarely seen in the datasheet. Unlike silicon MOSFET, GaN doesn’t have avalanche breakdown. Once GaN device breakdown, the device is destroyed, and the equipment is likely not fast enough to catch the complete curves.

- GaNPower’s 650V E-mode devices real breakdown voltage is above 900V for a safety margin.

- GaNPower is also the world’s first and only provider of 1200V single chip E-mode GaN HEMT, with real breakdown voltage exceeding 1500V.
Parameter Testing: $R_g$

Gate internal resistance is measured with drain open and high frequency, such as $f=25\text{MHz}$

\[ V(t) = V_{bias} + V_o \sin \omega t \]
\[ I(t) = I_o \sin(\omega t + \theta) \]
\[ I_o = \frac{V_o}{\sqrt{R^2 + \left(\frac{1}{\omega C}\right)^2}} \]
\[ \theta = \tan^{-1}\frac{1}{R \omega C} \]
Parameter Testing: $R_{dson}$ vs. Temp

For GaN HEMT: $R_{dson}$ temp ratio: $R_{dson(T=25°C)} / R_{dson(T=150°C)} = 195\,\text{mΩ} / 92\,\text{mΩ} = 2.12$

For SJ MOS: $R_{dson}$ temp ratio: $R_{dson(T=25°C)} / R_{dson(T=150°C)} = 200\,\text{mΩ} / 90\,\text{mΩ} = 2.17$

$R_{dson}$ temperature ratio of GaN HEMT and SJ MOS are on par
Parameter Testing: $I_D$ vs. $V_{GS}$

For silicon SJ MOS, a Zero Temperature Coefficient (ZTC) point exists. Below this point, current increases with increasing temperature, causing hot spot and device failure. E-mode GaN has no such issue.
Parameter Testing: $V_{th}$ vs. Temp

Typical GaN $V_{th}$ vs. Temperature

E-mode GaN 650V 50 mΩ

Threshold Voltage vs Temp.

Typical SiC $V_{th}$ vs. Temperature

Gangyao Wang, John Mookken, Julius Rice, Marcelo Schupbach: Dynamic and Static Behavior of Packaged Silicon Carbide MOSFETs in Paralleled Applications, IEEE
https://www.richardsonrfpd.com/docs/rfpd/Dynamic_and_Static_Behavior_SiC_MOSFET.pdf
Parameter Testing: Reverse Cond. and $V_{sd}$

- There is no PN junction in the GaN device
- With $S$ and $G$ connected, applying a negative $V_{DS}$ equals to applying a positive $V_{GD}$
- When $V_{GD}$ exceeds the threshold voltage, the channel will conduct current, much like the body-diode of a MOSFET
- A negative bias on the Gate terminal requires an equal potential drop on the drain terminal so that $V_{GD}$ can reach $V_{th}$
- In datasheet, $V_{sd}$ is usually larger than $V_{th}$ because the test criteria of $I_d$ (for $V_{th}$) and $I_s$ (for $V_{sd}$) is different. $V_{sd}$ is usually defined at a much higher current value than $V_{th}$
Parameter Testing: Capacitance

\[ C_{iss} = C_{GS} + C_{GD} \]
\[ C_{oss} = C_{DS} + C_{GD} \]
\[ C_{rss} = C_{GD} \]
Parameter Testing: Capacitance

\[ C_{\text{oss}} = \frac{C_{\text{isolation}}}{C_{\text{isolation}} - C_{\text{measured}}} \]
\[ C_{\text{measured}} \ll C_{\text{isolation}} = 1\mu F; \quad C_{\text{measured}} \sim pF \text{ range} \]
\[ C_{\text{iss}} \approx C_{\text{measured}} \]

\[ C_{\text{rss}} = \frac{C_{\text{isolation}}}{C_{\text{isolation}} - C_{\text{measured}}} \]
\[ C_{\text{measured}} \ll C_{\text{isolation}} = 1\mu F; \quad C_{\text{measured}} \sim pF \text{ range} \]
\[ C_{\text{rss}} \approx C_{\text{measured}} \]
Capacitance: **Si SJ MOS vs. GaN**

For GaN HEMT: $C_{\text{OSS}}$ variation: $C_{\text{OSS}}(V_{\text{ds}}=0.5\text{V})/C_{\text{OSS}}(V_{\text{ds}}=500\text{V})=521\text{pF}/30\text{pF}=17.4$

For Si SJ MOS: $C_{\text{OSS}}$ variation: $C_{\text{OSS}}(V_{\text{ds}}=0.5\text{V})/C_{\text{OSS}}(V_{\text{ds}}=500\text{V})=2.8\times10^4\text{pF}/32\text{pF}=875$

Silicon SJ MOSFET has a much wider $C_{\text{OSS}}$ variation, which causes significant non-linearity -> more severe EMI
Super Junction MOS $C_{DS}$ Non-linearity

- $C_{ds}$ can be calculated as:
  
  \[ C_{ds} \propto \frac{\varepsilon A}{d} \]

- $A$ is the total area formed by the P/N junction depletion region, $d$ is depletion width

- For small $V_{ds}$, $A$ is large, and $d$ is narrow, so $C_{ds}$ is large

- With increasing $V_{ds}$, $d$ increases while $A$ keeps almost constant, $C_{ds}$ decreases

- At certain $V_{ds}$, the lateral depletion regions merge, $A$ suddenly drops, and $d$ is wide, $C_{ds}$ decreases significantly
GaN $C_{GD}$ Non-linearity

$C_{GD}$ of GaN can be viewed as $C_{GD1}$ and $C_{GD3}$ in series and $C_{GD2}$ in parallel:

$$C_{GD} = C_{GD1} + \frac{C_{GD2}C_{GD3}}{C_{GD2} + C_{GD3}}$$

With a high $V_{DS}$ applied, while $C_{GD1}$ and $C_{GD2}$ are not sensitive to $V_{DS}$, $C_{GD3}$ decreases with the increasing depletion region, causing $C_{GD}$ to decrease.

The nonlinearity of GaN is much smaller than SJ MOS in terms of $C_{GD}$ and $C_{DS}$.
Capacitance: $C_{o(\text{er})}$ and $C_{o(\text{tr})}$

- $C_{\text{oss}}$ is voltage dependent, no matter GaN or SJ MOS

- Single point $C_{\text{oss}}$ value is not very useful, it can’t represent the entirety of the capacitance curve

- By using the energy and time related effective output capacitance values, calculations will be more accurate, and they are more convenient to use

- These output capacitances ($C_{o(\text{er})}$ and $C_{o(\text{tr})}$) are usually evaluated at 80% of rated breakdown voltage (80% $\text{BV}_{\text{dss}}$, or $\text{BV}_{80\%}$)

- The energy related effective output capacitance $C_{o(\text{er})}$ and time related effective output capacitance $C_{o(\text{tr})}$ can be calculated using the following equations:

$$C_{o(\text{tr})} = \frac{Q_{\text{oss}} - 80\%}{\text{BV}_{80\%}} = \frac{\int_{0}^{\text{BV}_{80\%}} C(V) dV}{\text{BV}_{80\%}}$$

$$C_{o(\text{er})} = \frac{2}{\text{BV}_{80\%}^2} = \int_{0}^{\text{BV}_{80\%}} C(V) V dV$$

Alexander J. Young, ON Semiconductor, Characterizing the dynamic output capacitance of a MOSFET
Parameter Testing: $Q_g$

- $Q_g$ can be tested with single pulse inductive load switching

- The value of $R_G$ is intentionally chosen to be large (>300Ω) so that the switching transient can be slowed down for better calculation

- $Q_g$ can then be extracted as (for Turn-off):
  
  \[
  I_G(t) = \frac{V_G(t) - V_G-\text{applied}(t)}{R_G}
  \]

  \[
  Q_G(V_G) = \int_0^t \frac{V_G(t) - V_G-\text{applied}(t)}{R_G} \, dt
  \]

  \[
  Q_{GS} = Q_G \left( V_G = V_{Plateau} \right)
  \]

  \[
  Q_{GD} = Q_G(V_D=0) - Q_G(V_D=V_{DD})
  \]
Parameter Testing: $Q_g$ Curve

GPI65015TO 92mΩ

Si SJ MOS 650V 95mΩ

$V_{ds} = 400\text{V}$

$I_d = 7.5\text{A}$

$V_{gs} = 6\text{V}$

GaN $Q_g$ is one order of magnitude smaller compared to silicon SJ MOS with similar $R_{ds}on$ and BV ratings.
Parameter Testing: $I_{dss}$ and $I_{gss}$ vs. Temp.

- **Gate Leakage $I_{GSS}$ vs. Temp**
  - GaNPower GPI65030DFN

- **Drain Leakage $I_{DSS}$ vs. Temp**
  - GaNPower GPI65015DFN

- 30A GIT GaN $I_g$ vs. $V_g$

- A GIT device, such as GaN offered by Panasonic and Infineon, exhibits a much higher gate current, since they are current driven, rather than voltage driven GaN devices, like BJTs.
Current Collapse: Dynamic $R_{\text{dson}}$

- There are various ways to measure dynamic $R_{\text{dson}}$, most of these methods involve a fast and accurate clamping circuit.

- In this setup, the voltage drop $V_{\text{clamp}}$ across the Zener diode $D_Z$ is measured instead of $V_{DS}$, the diode forward voltage $V_{D1}$ is calibrated so that low $R_{\text{dson}}$ of GaN can be accurately measured.

- $R$ is chosen to limit the current of $D_1$ so that it won’t heat-up.

Current Collapse: Dynamic $R_{dson}$

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Device A</th>
<th>Device B</th>
<th>Device C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage/Current Rating</td>
<td>600V/13A</td>
<td>650V/30A</td>
<td>600V/35A</td>
</tr>
<tr>
<td>Technology</td>
<td>E-mode (X-GaN GIT)</td>
<td>E-mode (p-gate)</td>
<td>CoolMOS™</td>
</tr>
<tr>
<td>Package</td>
<td>DFN 8×8</td>
<td>GaNPX™ 4</td>
<td>TO-220</td>
</tr>
<tr>
<td>$R_{DSON}^a$</td>
<td>140mΩ</td>
<td>50mΩ</td>
<td>60mΩ</td>
</tr>
</tbody>
</table>

Technology has improved over the past two years, the dynamic $R_{dson}$ is better now than 2 years ago.

Source: Rui Li, Xinke Wu, Gang Xie, Kuang Sheng, Dynamic On-state Resistance Evaluation of GaN Devices under Hard and Soft Switching Conditions, APEC 2018
Parameter Testing: Thermal Resistance

➢ To test the thermal resistance, we need to know the accurate junction temperature within the packaged device. (We can test the junction temperature using thermal imager or thermal coupler, but it needs to teardown the case)

➢ For MOSFET with PN junctions, body diode forward voltage $V_f$ is monitored for sensing the junction temperature. GaN has no body diode. Instead, $R_{dson}$ is used to sense the $T_j$, which means $T_j = T_j(R_{on})$

$$R_{\theta jc}(t) = \frac{T_j - T_c}{P(t)} = \frac{T_j(R_{on}) - T_c}{\int_0^t V_d(t)I_d(t)dt} = \frac{T_j(V_d(t)/I_d(t)) - T_c}{\int_0^t V_d(t)I_d(t)dt}$$

![Diagram of MOSFET with voltage and current waveforms](image)
$R_{\text{thJC}}$ from Various Packaging Forms

<table>
<thead>
<tr>
<th>Package Type</th>
<th>$R_{\text{dson}}$</th>
<th>Material</th>
<th>$R_{\text{thJC}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPP65R065C7</td>
<td>65mΩ/33A</td>
<td>Si</td>
<td>0.73 K/W</td>
</tr>
<tr>
<td>IPL65R070C7</td>
<td>ThinPAK 8x8</td>
<td>Si</td>
<td>0.74 K/W</td>
</tr>
<tr>
<td>IPW60R060P7</td>
<td>TO247</td>
<td>Si</td>
<td>0.76 K/W</td>
</tr>
<tr>
<td>IPB65R065C7</td>
<td>TO263</td>
<td>Si</td>
<td>0.73 K/W</td>
</tr>
<tr>
<td>IGLD60R070D1</td>
<td>DFN 8x8</td>
<td>GaN</td>
<td>1.1 K/W</td>
</tr>
</tbody>
</table>

All data from Infineon datasheet
Parameter Testing: **Thermal Impedance**

- **Thermal resistor** determines how much power it will dissipate for certain temperature change, while **thermal capacitor** governs the thermal capacity, or how much heat it can hold on.

- Sometimes in **Failure Analysis**, we use thermal impedance as a guideline for damage caused by either **Temperature Cycling (TC)** or **Power Cycling (PoC)**. TC tests how the external temperature impact device life-time, while PoC tests how the self-heating gradually damage the device internally.
Parameter Testing: Transient Thermal Impedance

- DC thermal impedance is the maximum thermal impedance at steady state.
- The transient thermal impedance is a measure of how the device behaves when pulsed power is applied to it. This is important for determining the behavior of low duty cycle, low frequency pulsed loads.
- For the same power level, at short durations, the thermal impedance appears to be smaller.

How to Rate Continuous Current?

- $I_{ds}$ calculated from this method reflects the upper current limit. To keep a safety margin, the current rating is usually lower than the calculated value.

- As an example, for CoolMOS IPB65R095C7, $R_{dson@T_{Jmax}}=0.202$, $R_{thJC}=0.98$, $I_{dsmax}$ from the above equation calculated as 25.13A. This device is rated as 24A by Infineon.

- Another current limiting factor is bond wire fusing. But most of the time bonding wires fuse only when devices fail.
Why GaN has a lower current rating with same $R_{\text{dson}}$?

- With the same packaging forms and similar $R_{\text{dson}}$, the continuous current of GaN is rated much lower than silicon, due to the fact that with the same $R_{\text{dson}}$, GaN chip size is usually much smaller than silicon counterpart, which increases thermal resistance $R_{\text{thJC}}$

- As an example, for a GaN device with $R_{\text{dson@TJmax}}=0.26\Omega$, $R_{\text{thJC}}=1.0\text{K/W}$, $I_{\text{dmax}}$ from the above equation calculated as 22A. This device is rated as 15A by the GaN manufacturer for some safety margins

- Also, the total area of lead-frame bonding pads determine how many bonding wires with certain thickness (1mil, 2mil?) can be applied. These bonding wires have limited current handling capabilities and can be the bottleneck for some packaging types (such as DFN)

- For GaN manufacturers such as GaNPower, we use the same chip in different packaging forms (such as TO220, DFN, etc...), the current ratings are always less meaningful than $R_{\text{dson}}$ values
How to Rate Pulsed Current

- The rating of max pulsed current is similar to that of a continuous current in that both current ratings are calculated rather than tested.

- The pulsed current rating is based on the current pulse duration and duty cycle specified (e.g. 100us duration and duty cycle=1%), with regard to the transient thermal impedance

\[
I_{ds\text{max}} = \sqrt{\frac{T_{J\text{max}} - T_c}{R_{dson@T_{J\text{max}}} R_{\theta JC} Z_{\theta JC}}}
\]

https://e2e.ti.com/blogs_/b/powerhouse/archive/2015/06/29/understanding-mosfet-data-sheets-part-4-mosfet-switching-times
**Chip Sizes Compared**

<table>
<thead>
<tr>
<th>Type</th>
<th>Current</th>
<th>Die Size</th>
<th>Rdson</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDMOS</td>
<td>10A</td>
<td>~21.6 mm²</td>
<td>0.65 Ω</td>
</tr>
<tr>
<td>SJ MOS Gen.1</td>
<td>10A</td>
<td>~12 mm²</td>
<td>0.35 Ω</td>
</tr>
<tr>
<td>SJ MOS Gen.1</td>
<td>10A</td>
<td>~8.6 mm²</td>
<td>0.38 Ω</td>
</tr>
<tr>
<td>SJ MOS Gen.1</td>
<td>10A</td>
<td>~5.6 mm²</td>
<td>0.38 Ω</td>
</tr>
<tr>
<td>GaN</td>
<td>10A</td>
<td>~4 mm²</td>
<td>0.13 Ω</td>
</tr>
</tbody>
</table>

- SJ Chip size shrinks during the past 20 years. However, **GaN is a quantum leap, even with lateral structures**.
- Smaller chip size means lower cost for the same technology.
FOM Comparison (SJ MOS vs. GaN)

FOM ($R_{dson} \cdot Q_g$) ($\Omega \cdot $ nC)

- SJ MOS Gen 1 (600V/0.19Ω): 16.5
- SJ MOS Gen 2 (600V/0.19Ω): 12
- SJ MOS Gen 2.5 (600V/0.19Ω): 6.4
- SJ MOS Gen 3 (600V/0.18Ω): 4.3
- GaN HEMT (650V/0.22Ω): 0.37
Parameter Testing: SOA

- GaN has similar SOA definition as Silicon devices
- The thermal instability region indicates where thermal runaway can occur, and the steeper the slope, the more prone the FET is to enter this thermal runaway condition at higher breakdown voltages
- TLP (Transmission Line Pulse) can be used to test the device SOA boundary

https://e2e.ti.com/b/powerhouse/archive/2015/05/02/understanding-mosfet-data-sheets-part-2-safe-operating-area-soa-graph Datasheet
www.transphormusa.com
Parameter Testing: Power Ratings

- With $R_{thJC}$ available, we can use this equation to calculate the max power allowed:

$$P_{max} = \frac{T_{Jmax} - T_c}{R_{thJC}}$$

- A power vs. case temperature curve can then be drawn based on the equation above

Reference: GaN Systems Datasheet

$R_{thjc}$ = 1 K/W
Datasheet Testing: Keysight B1505A/B1506A

- Keysight 1500 series is a one stop power device parameter testing platform, with All-in-one solution for power device characterization up to 1500A/10kV
  - Fully automated Capacitance ($C_{iss}$, $C_{oss}$, $C_{rss}$, etc.) measurement at up to 3000V of DC bias
  - Gate charge measurement
  - High voltage/high current fast switch option to characterize GaN current collapse effect
  - Perform both hot and cold temperature dependency testing in an interlock equipped test fixture

Source: https://www.keysight.com/
Double Pulse Tests: Methods

- The load inductor is used to establish the desired current during the first pulse and keep this current nearly constant during the subsequent turn-off and turn-on transients.

- The capacitors are employed to maintain a stable DC bus voltage. Bulk capacitors with large capacitance supplies energy to establish the inductive current during the first pulse, while the decoupling capacitor with low parasitic equivalent series inductance (ESL) is responsible for supplying transient current during the switching transition.

- A bleeder resistor is introduced across the DC bus to dissipate the remaining energy stored at the DC capacitors.

- The DPT signals are generated either by a signal generator or by a MCU.

Source: Fei (Fred) Wang, Zheyu Zhang, and Edward A. Jones, Characterization of Wide Bandgap Power Semiconductor Devices; published by The Institution of Engineering and Technology 2018
Double Pulse Tests: Descriptions

- With a constant voltage and a given inductor in the test, there is a constant current change rate $\frac{di}{dt}$ during turn-on.

- The width of the first pulse is set to achieve the current you want to observe, for device characterization this often is the device's rated current.

- At the end of the first pulse, the double pulse test allows to observe "turn-off rated current".

- The current commutates to the freewheeling diode and gets back to the GaN when turning on the second pulse. An oscilloscope properly set will observe "turn-on of rated current" at the rising edge of the second pulse. However, during the turn-on period, the current in the device grows and does so exceeding the rated current. As everything you want to learn takes place during the rising edge, the second pulse can be as short as possible.

- The important parts are the falling edge of pulse one and the rising edge of pulse two.

Double Pulse Tests: Some Tips

- In DPT, it is important to have a low inductance loop to minimize the $V_{ds}$ voltage overshoot.

- For current measurement, a current probe requires additional wiring, which brings high frequency inductance. It is necessary to insert a dynamic current measurement, typically coaxial shunt, into the switching loop.

- Gate loop is not from the gate drive IC to the device, but from the gate drive decoupling capacitor to gate drive IC and then the device. Magnetic field cancellation concept can be used to minimize the gate loop parasitics.
Contents

- Session 1: GaN devices basics
  - GaN, An Introduction
  - GaN Design, Fabrication and Testing
  - GaN Compact Modeling and Reliability
- Session 2: GaN Gate Driving
- Session 3: GaN Applications
Compact Modeling of GaN HEMT

- There are three compact modeling methods: physics-based, semiphysics-based or behavioral model.

- The physics-based model is based on the physical structure and internal parameters of GaN HEMT, which is very accurate, however, it's not suitable for power electronics circuit simulations due to the complicated physical parameter extraction process, as well as the long simulation time.

- Semiphysics-based model is partly based on the physical structure and internal parameters of GaN HEMT, and some behavioral equations are included.

- Behavioral model is mainly based on behavioral equations of GaN HEMT, the information about the physical structure and the internal parameters of GaN HEMT is not necessary any more.

Hong Li, Xingran Zhao, Wenzhe Su, Kai Sun, Trillion Q. Zheng and Xiaojie You; Non-segmented PSpice Circuit Model of GaN HEMT with Simulation Convergence Consideration, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS 2017
Compact Modeling of GaN HEMT: Behavioral model Example

- For static modeling that takes temperature into account:

\[
I_{DS} = K_1(T) \cdot \ln[1 + \exp\left(\frac{V_{GS} - b_1}{c_1}\right)] \\
\cdot \frac{(m_1 + n_1 \cdot V_{GS})V_{DS}}{1 + P_1(T) \cdot (d_1 + e_1 \cdot V_{GS})V_{DS}}, \quad V_{DS} > 0 \\
I_{DS} = -K_2(T) \cdot \ln[1 + \exp\left(\frac{V_{GD} - b_2}{c_2}\right)] \\
\cdot \frac{V_{SD}}{1 + P_1(T) \cdot V_{SD}}, \quad V_{DS} \leq 0
\]

\[
K_1(T) = K_1 \cdot [1 - l_1 \cdot (T - 25)] \\
K_2(T) = K_2 \cdot [1 - l_2 \cdot (T - 25)] \\
P_1(T) = [1 - h_1 \cdot (T - 25)] \\
P_2(T) = [1 - h_2 \cdot (T - 25)]
\]

- For dynamic modeling that takes temperature into account:

- Model parameters are extracted with measurement data

Hong Li, Xingran Zhao, Wenzhe Su, Kai Sun, Trillion Q. Zheng and Xiaojie You; Non-segmented PSpice Circuit Model of GaN HEMT with Simulation Convergence Consideration, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS 2017
Compact Modeling of GaN HEMT: Behavioral model Example

- In order to have an accurate simulation, all the parasitics in the circuitry should be included. The numbers can be extracted from either measurements or 3D structural simulations such as Ansoft Q3D:

- Good fits can be obtained from proper parameter extraction for the behavior compact model:

Hong Li, Xingran Zhao, Wenzhe Su, Kai Sun, Trillion Q. Zheng and Xiaojie You; Non-segmented PSpice Circuit Model of GaN HEMT with Simulation Convergence Consideration, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS 2017
Compact Modeling of GaN HEMT: Behavioral model Example

- Similar modeling method (behavioral model) is also provided by Keysight technologies:
  - Measured device characteristics turned into mathematical representation
  - Accurately represents device behavior which can’t be achieved with any physics-based model
  - Less parameters with better conversion
  - Independent of device physics parameters (e.g. $T_{ox}$) → Everyone (e.g. circuit designer) can use

\[
\tanh \left( \left( \text{Lambda1} \times \tanh(1 + \text{Lambda2} \times V_{gs}) \right) \times V_{ds} \right)
\]

Added $V_{gs}$, $V_{ds}$ dependent parameter to drain current equation to better represent unsaturated drain current

\[
Q_{gs} = (C_{gspl} + C_{gs0} \times \tanh(02)) + (C_{gspl} + (C_{gs0} \times \tanh(01) + C_{gs0i} \times \tanh(1i)) \times \tanh(02))
\]

\[
tanhXX(t) = 1 + \tanh(A + B \times V_{gs} + C \times V_{ds})
\]

Added $tanhXX$ to express a positive bias dependence on charge equation
Reliability Testing: Bathtub Curve

- **Infant Mortality**: (Decreasing Failure Rate)
- **Useful Life**: (Random Failures)
- **Wear Out**: (Beyond Product Lifetime)
Reliability Testing: Examples

A typical JEDEC standard reliability tests for power devices should cover a long list of items, here is a highly simplified version to show some of the tested items.

<table>
<thead>
<tr>
<th>Test Items</th>
<th>Description</th>
<th>Requirements</th>
<th>Number of Chips from 3 lots each</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTGB</td>
<td>High Temperature Gate Bias</td>
<td>168h</td>
<td>77</td>
</tr>
<tr>
<td>HTRB</td>
<td>High Temperature Reverse Bias</td>
<td>168h</td>
<td>77</td>
</tr>
<tr>
<td>Temp. Cycles</td>
<td>Temperature Cycling Tests</td>
<td>-65°C / +150°C, 500 cycles, dwell time: 10-15minutes</td>
<td>77</td>
</tr>
<tr>
<td>PCT</td>
<td>Pressure Cooker Test</td>
<td>96h,T=121°C ; RH=100%</td>
<td>77</td>
</tr>
<tr>
<td>THB</td>
<td>Temperature, Humidity, Bias Tests</td>
<td>1000h with bias</td>
<td>77</td>
</tr>
<tr>
<td>HTS</td>
<td>High Temperature Storage</td>
<td>150°C , 1000hrs</td>
<td>77</td>
</tr>
</tbody>
</table>
Reliability Testing: JC-70

A new JEDEC committee: JC-70 was established in 2017 to deal specifically for wide bandgap devices reliability issues. A sample proposed items for guidelines is listed below:

<table>
<thead>
<tr>
<th>REL</th>
<th>Test</th>
<th>Datasheet</th>
</tr>
</thead>
<tbody>
<tr>
<td>• List of Failure Mechanisms &amp; Resulting Failure Mode</td>
<td>• Dynamic $R_{DS(ON)}$&lt;br&gt;• Thermal Resistance (only for cascodes)&lt;br&gt;• Safe Operating Area (SOA)</td>
<td>• Include effect of Dynamic $R_{DS(ON)}$&lt;br&gt;• Nomenclature of parameters to adjust for uniqueness of GaN power transistors&lt;br&gt;• Transistor circuit symbol to reflect distinctive operation GaN HEMTs</td>
</tr>
<tr>
<td>• Focusing on Charge Trapping, Charge Injection, Hot Electron, Corrosion, TDDB Like Mechanism, Delam</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Corresponding Acceleration &amp; Stress Procedure</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Update: JEP173: Dynamic On-Resistance Test Method Guidelines for GaN HEMT Based Power Conversion Devices was released in 2019

Status of wide bandgap device qualification standards effort by new JEDEC committee JC70, APEC 2018
ISO, RoHS and IATF16949

- **ISO** is the basic requirement for semiconductor manufactures and packaging houses.

- **RoHS** (Restriction of Hazardous Substances) is generally required.

- **IATF16949** is one of the automotive industry’s most widely used international standards for quality management.

- For fabless design house such as GaNPower, we rely on our foundry and packaging partners for these certificates

An example of RoHS test certificate

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THANKS FOR WATCHING!

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