GaNPower International Inc.

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230 -3410 LOUGHEED HWY
VANCOUVER, BC, V5M 2A4 CANADA

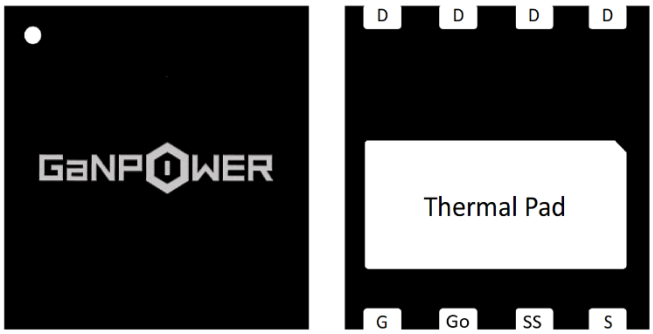
GPI65030DSOVP

Gate-Protected 650 V, 30 A GaN Power HEMT in 8x8 DFN package
Proof of concept design; Preliminary engineering samples

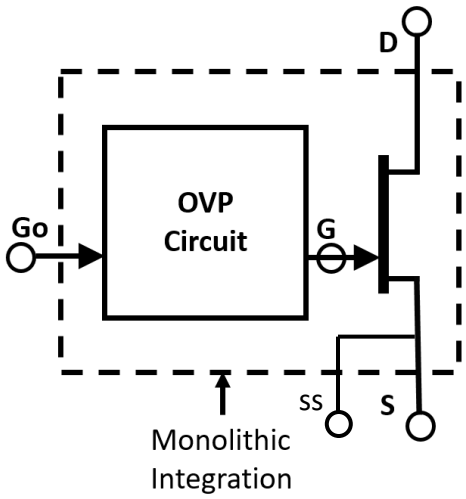
Datasheet — Testing data (Preliminary)

Features

Order Code	V_{dss}	$R_{dson)}$	I_d
GPI65030DSOVP	650 V	55 mΩ	30 A



- Ultra-low $R_{DS(on)}$
- High dv/dt capability
- Extremely low input capacitance
- Zero Qrr
- Gate over-voltage protection (OVP) up to 100V
- Wider gate driving range up to 15V
- Outstanding switching performance



Applications

- Switching Power Applications

Description

These devices are N-channel 650 V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology. The resulting product has extremely low on state resistance, very low input capacitance and zero reverse recovery charge making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency. Over-voltage protection (OVP) circuit clamps the input gate driving voltage to below about 8 volt for safe operation. The OVP also makes it feasible to drive the transistor for a wider gate driving voltage of 5-15V. Monolithic integration reduces parasitic effects due to the OVP circuit.

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Static Parameters					
				Typical data	
NO.	**Parameters**		**Condition**	**1#**	**Unit**
1	$V_{gs(TH)}$	Gate Threshold Voltage	V_{ds}=V_{gs} Id=4.6mA	1.3	V
2	BV_{dss}	Drain-Source breakdown voltage	V_{gs}=0V I_d=25uA	>650	V
3	I_{dss}	Zero gate voltage drain current, T_C = 25℃	V_{gs}=0V V_{ds}=650V	0.635	uA
4	I_{gss}	Gate-Source Leakage	V_{gs} = 6V V_{ds} =0V	48.54	uA
5	R_{dson}	static Drain-Source on resistance, T_C = 25℃	V_{gs}=6V I_d=7.5A	0.055	Ω
6	V_{sd}	Reverse conduction voltage	I_{sd}=1A V_{gs}=0V	1.83	V
Dynamic Parameters				**Typical data**	**Unit**
1	capacitance	C_{iss}	V_{gs}=0V V_{ds}=400V f=1MHz	241	pf
		C_{oss}		61	pf
		C_{rss}		8.4	pf
3	Q_g	Gate charge	V_{ds}=400V I_d=9A V_{gs}=6V	5.8	nC
	Q_{gS}			1.2	nC
	Q_{gd}			1.5	nC
Switching Performance				**Test data**	**Unit**
1	$t_{d(on)}$	Turn-on delay time	V_{ds}=400V I_d=2.5A R_g=10Ω V_{gs}=6V	6	ns
2	t_r	Rise time		12	ns
3	$t_{d(off)}$	Turn-off delay time		15	ns
4	t_f	Fall time		13	ns

Output Curve (Id vs. Vd family of curves @ 25C)

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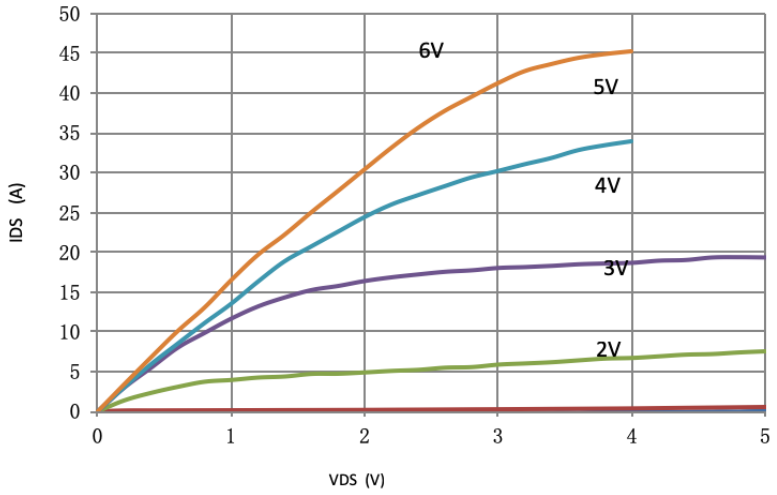
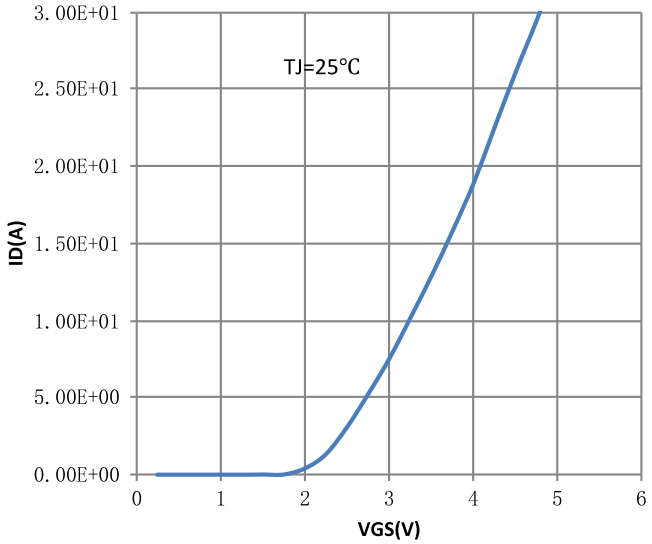


Transfer Curve (Id vs. Vg @25C)



Rdson (Ron vs. Id pulsed)

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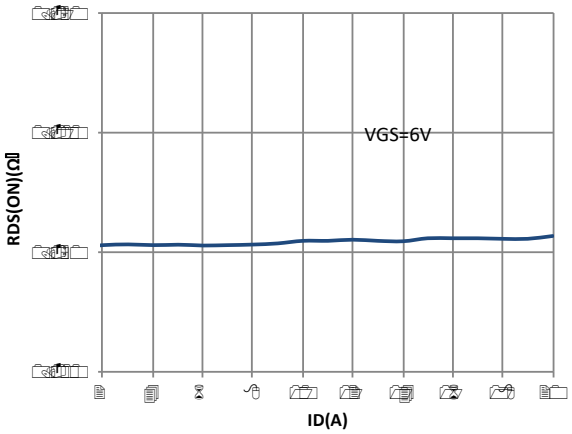
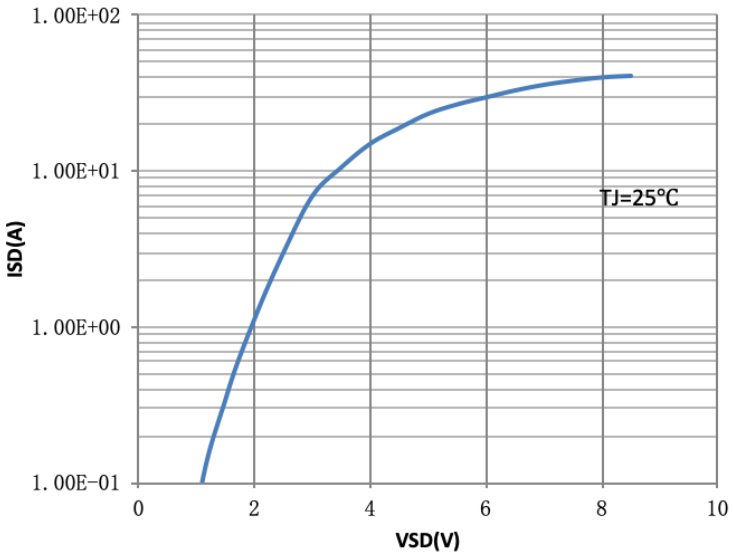


Reverse conduction (Isd vs. Vsd)



Capacitance

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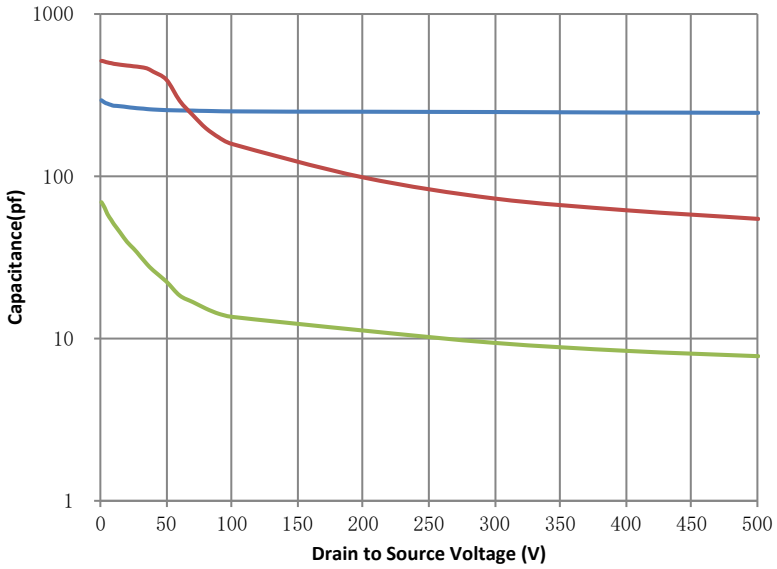
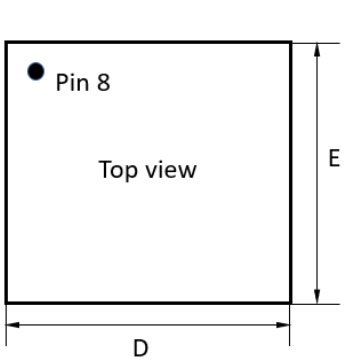


Packaging Information

DFN8x8 OVP-GaN: Suggested driving range G: 5-6V; GO: 5-15V, protection > 30V



D=8; E=8; e=1.95; b=0.97; L=0.57; D2=6.82; E2=3.19

8LEAD DFN (8x8x0.75mm, Pitch 1.95mm)
IMPORTANT:Please connect the bottom thermal pad to the source electrode on PCB